19-3131; Rev 0; 3/08

50MHz to 1000MHz High-Linearity, Serial/ Parallel-Controlled Analog/Digital VGA

MAX2065

General Description

The MAX2065 high-linearity, analog/digital variable-gain amplifier (VGA) is designed to operate in the 50MHz to 1000MHz frequency range with two independent attenuators (see the *Typical Application Circuit*). The digital attenuator is controlled as a slave peripheral using either the SPI™-compatible interface or a parallel bus with 31dB total adjustment range in 1dB steps. An added feature allows "rapid-fire" gain selection between each of four steps, preprogrammed by the user through the SPI-compatible interface. The 2-pin control allows the user to quickly access any one of four customized attenuation states without reprogramming the SPI bus. The analog attenuator is controlled using an external voltage or through the SPI-compatible interface using an on-chip 8-bit DAC.

Because each of the three stages has its own RF input and RF output, this component can be configured to either optimize NF (amplifier configured first), OIP3 (amplifier last), or a compromise of NF and OIP3. The device's performance features include 22dB amplifier gain (amplifier only), 6.5dB NF at maximum gain (includes attenuator insertion losses), and a high OIP3 level of +42dBm. Each of these features makes the MAX2065 an ideal VGA for numerous receiver and transmitter applications.

In addition, the MAX2065 operates from a single +5V supply with full performance, or a single +3.3V supply with slightly reduced performance, and has an adjustable bias to trade current consumption for linearity performance. This device is available in a compact 40-pin thin QFN package (6mm x 6mm) with an exposed pad. Electrical performance is guaranteed over the extended temperature range (T_C = -40°C to +85°C).

Applications

- IF and RF Gain Stages
- Temperature Compensation Circuits
- Cellular Band WCDMA and cdma2000® Base Stations
- GSM 850/GSM 900 EDGE Base Stations
- WiMAX and LTE Base Stations and Customer Premise Equipment
- Fixed Broadband Wireless Access
- Wireless Local Loop
- Military Systems
- Video-on-Demand (VOD) and DOCSIS®-Compliant EDGE QAM Modulation
- Cable Modem Termination Systems (CMTS)

SPI is a trademark of Motorola, Inc.

Features

- **50MHz to 1000MHz RF Frequency Range**
- **Pin-Compatible Family Includes:**
  - **MAX2066 (Digital VGA)**
  - **MAX2067 (Analog VGA)**
- **+19.4dB (Typ) Maximum Gain**
- **0.5dB Gain Flatness Over 100MHz Bandwidth**
- **62dB Gain Range (31dB Analog + 31dB Digital)**
- **Built-in DAC for Analog Attenuation Control**
- **Supports Four "Rapid-Fire" Preprogrammed Attenuator States**
  - **Quickly Access Any One of Four Customized Attenuation States Without Reprogramming the SPI Bus**
  - **Ideal for Fast-Attack, High-Level Blocker Protection**
  - **Prevents ADC Overdrive Condition**
- **Excellent Linearity (Configured with Amplifier Last)**
  - **+42dBm OIP3**
  - **+63dBm OIP2**
  - **+19dBm Output 1dB Compression Point**
  - **-67dBc HD2**
  - **-83dBc HD3**
- **6.5dB Typical Noise Figure (NF)**
- **Fast, 25ns Digital Switching**
- **Very Low Digital VGA Amplitude Overshoot/ Undershoot**
- **Single +5V Supply (Optional +3.3V Operation)**
- **External Current-Setting Resistors Provide Option for Operating Device in Reduced-Power/ Reduced-Performance Mode**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX2065ETL+	-40°C to +85°C	40 Thin QFN-EP*	T4066-3
MAX2065ETL+T	-40°C to +85°C	40 Thin QFN-EP*	T4066-3

+Denotes a lead-free package.
**EP = Exposed pad.*
T = Tape and reel.

Pin Configuration appears at end of data sheet.

cdma2000 is a registered trademark of Telecommunications Industry Association.

DOCSIS and CableLabs are registered trademarks of Cable Television Laboratories, Inc. (CableLabs®).

50MHz to 1000MHz High-Linearity, Serial/ Parallel-Controlled Analog/Digital VGA

ABSOLUTE MAXIMUM RATINGS

VCC_ to GND ....-0.3V to +5.5V
VDD_LOGIC, DATA, $\overline{CS}$, CLK, SER/PAR, VDAC_EN,
VREF_SELECT....................................-0.3V to (VCC_ + 0.3V)
STATE_A, STATE_B, D0–D4....................-0.3V to (VCC_ + 0.3V)
AMP_IN, AMP_OUT, VREF_IN,
ANALOG_VCTRL ....-0.3V to (VCC_ + 0.3V)
ATTEN1_IN, ATTEN1_OUT, ATTEN2_IN,
ATTEN2_OUT..-1.2V to + 1.2V
RSET to GND...-0.3V to + 1.2V

RF Input Power (ATTEN1_IN, ATTEN1_OUT,
ATTEN2_IN, ATTEN2_OUT)......................................+20dBm
RF Input Power (AMP_IN)..+18dBm
Continuous Power Dissipation (Note 1) 6.5W
θ_{JA} (Notes 2, 3)...+38°C/W
θ_{JC} (Note 3) ....+10°C/W
Operating Temperature Range (Note 4).....T_C = -40°C to +85°C
Maximum Junction Temperature ....+150°C
Storage Temperature..-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Note 1: Based on junction temperature $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$. This formula can be used when the temperature of the exposed pad is known while the device is soldered down to a printed-circuit board (PCB). See the *Applications Information* section for details. The junction temperature must not exceed +150°C.

Note 2: Junction temperature $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$. This formula can be used when the ambient temperature of the PCB is known. The junction temperature must not exceed +150°C.

Note 3: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a 4-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Note 4: T_C is the temperature on the exposed pad of the package. T_A is the ambient temperature of the device and PCB.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

+3.3V SUPPLY DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, high-current (HC) mode, V_{CC} = +3.0V to +3.6V, T_C = -40°C to +85°C. Typical values are at V_{CC} = +3.3V and T_C = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
Supply Current	I_{CC}			60	80	mA
LOGIC INPUTS (DATA, $\overline{CS}$, CLK, VDAC_EN, VREF_SELECT, SER/PAR, STATE_A, STATE_B, D0–D4)						
Input High Voltage	V_{IH}			2		V
Input Low Voltage	V_{IL}			0.8		V

+5V SUPPLY DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, V_{CC} = +4.75V to +5.25V, T_C = -40°C to +85°C. Typical values are at V_{CC} = +5V and T_C = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5	5.25	V
Supply Current	I_{CC}	Low-current (LC) mode		73	93	mA
		High-current (HC) mode		124	146	
LOGIC INPUTS (DATA, $\overline{CS}$, CLK, VDAC_EN, VREF_SELECT, SER/PAR, STATE_A, STATE_B, D0–D4)						
Input High Voltage	V_{IH}		3			V
Input Low Voltage	V_{IL}				0.8	V
Input Current Logic-High	I_{IH}		-1		+1	µA
Input Current Logic-Low	I_{IL}		-1		+1	µA

+3.3V SUPPLY AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, V_{CC} = +3.0V to +3.6V, T_C = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, HC mode with attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RF Frequency Range	f_{RF}	(Notes 6, 7)	50		1000	MHz
Small Signal Gain	G			18.8		dB
Output Third-Order Intercept Point	OIP3	P_{OUT} = 0dBm/tone, maximum gain setting		37.5		dBm
Noise Figure	NF	Maximum gain setting		6.7		dB
Total Attenuation Range		Analog and digital combined		61.5		dB

+5V SUPPLY AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, V_{CC} = +4.75 to +5.25V, HC mode with each attenuator set for maximum gain, 50MHz ≤ f_{RF} ≤ 1000MHz, T_C = -40°C to +85°C. Typical values are at V_{CC} = +5.0V, HC mode, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RF Frequency Range	f_{RF}	(Notes 6, 7)		50		1000	MHz
Small Signal Gain	G	200MHz			19.4		dB
		350MHz, T_C = +25°C		17.5	18.7	19.7	
		450MHz			18.2		
		750MHz			16.4		
		900MHz			15.6		
Gain Variation vs. Temperature					-0.006		dB/°C
Gain Flatness vs. Frequency		Any 100MHz frequency band from 50MHz to 500MHz			0.5		dB
Noise Figure	NF	200MHz			6.5		dB
		350MHz, T_C = +25°C (Note 7)			6.8	8	
		450MHz			7		
		750MHz			7.8		
		900MHz			8.2		
Total Attenuation Range		Analog and digital combined			61.5		dB
Output Second-Order Intercept Point	OIP2	P_{OUT} = 0dBm/tone, Δf = 1MHz, $f_1 + f_2$			63		dBm
Output Third-Order Intercept Point	OIP3	P_{OUT} = 0dBm/tone, HC mode, Δf = 1MHz	200MHz		42		dBm
			350MHz		40		
			450MHz		39		
			750MHz		36		
			900MHz		35		
		P_{OUT} = 0dBm/tone, LC mode, Δf = 1MHz	200MHz		40		
			350MHz		38		
			450MHz		37		
			750MHz		35		
			900MHz		33		

50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Analog/Digital VGA

+5V SUPPLY AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, V_{CC} = +4.75 to +5.25V, HC mode with each attenuator set for maximum gain, 50MHz ≤ f_{RF} ≤ 1000MHz, T_C = -40°C to +85°C. Typical values are at V_{CC} = +5.0V, HC mode, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output -1dB Compression Point	P_{1dB}	350MHz, T_C = +25°C (Note 8)		17	18.7		dBm
Second Harmonic		P_{OUT} = +3dBm, f_{RF} = 200MHz, T_C = +25°C (Note 7)		-60	-67		dBc
Third Harmonic		P_{OUT} = +3dBm, f_{RF} = 200MHz, T_C = +25°C (Note 7)		-71	-83		dBc
Input Return Loss		50Ω source, maximum gain setting			18		dB
Output Return Loss		50Ω load, maximum gain setting			18		dB
DIGITAL ATTENUATOR							
Insertion Loss					2.5		dB
Input Second-Order Intercept Point	IIP2	P_{RF1} = 0dBm, P_{RF2} = 0dBm, Δf = 1MHz, $f_1 + f_2$			52		dBm
Input Third-Order Intercept Point	IIP3	P_{RF1} = 0dBm, P_{RF2} = 0dBm, Δf = 1MHz			41		dBm
Attenuation Range					31.2		dB
Step Size					1		dB
Relative Step Accuracy					0.2		dB
Absolute Step Accuracy					0.45		dB
Insertion Phase Step		f_{RF} = 170MHz	0dB to 16dB		4.8		Degrees
			24dB		8		
			31dB		10.8		
Amplitude Overshoot/Undershoot		Between any two states	ET = 15ns		1.0		dB
			ET = 40ns		0.05		
Switching Speed		RF settled to within ±0.1dB	31dB to 0dB		25		ns
			0dB to 31dB		21		
Input Return Loss		50Ω source			19		dB
Output Return Loss		50Ω load			19		dB
ANALOG ATTENUATOR							
Insertion Loss					1.2		dB
Input Second-Order Intercept Point	IIP2	P_{RF1} = 0dBm, P_{RF2} = 0dBm, maximum gain setting, Δf = 1MHz, $f_1 + f_2$			70		dBm
Input Third-Order Intercept Point	IIP3	P_{RF1} = 0dBm, P_{RF2} = 0dBm, maximum gain setting, Δf = 1MHz			36		dBm
Attenuation Range		Analog control input			31.1		dB
Gain Control Slope		Analog control input			-12.5		dB/V
Maximum Gain Control Slope		Over analog control input range			-35		dB/V
Insertion Phase Change		Over analog control input range			18		Degrees
Group Delay		Maximum gain setting			0.98		ns
Group Delay vs. Control Voltage		Over analog control input range			-0.25		ns
Analog Control Input Range				0.25		2.75	V

+5V SUPPLY AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, V_{CC} = +4.75 to +5.25V, HC mode with each attenuator set for maximum gain, 50MHz ≤ f_{RF} ≤ 1000MHz, T_C = -40°C to +85°C. Typical values are at V_{CC} = +5.0V, HC mode, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Control Input Impedance				80		kΩ
Input Return Loss		50Ω source		22		dB
Output Return Loss		50Ω load		22		dB
D/A CONVERTER						
Number of Bits				8		Bits
Output Voltage		DAC code = 00000000			0.25	V
		DAC code = 11111111	2.75			
SERIAL PERIPHERAL INTERFACE (SPI)						
Maximum Clock Speed	f_{CLK}			20		MHz
Data-to-Clock Setup Time	t_{CS}			2		ns
Data-to-Clock Hold Time	t_{CH}			2.5		ns
Clock-to-$\overline{CS}$ Setup Time	t_{ES}			3		ns
$\overline{CS}$ Positive Pulse Width	t_{EW}			7		ns
$\overline{CS}$ Setup Time	t_{EWS}			3.5		ns
Clock Pulse Width	t_{CW}			5		ns

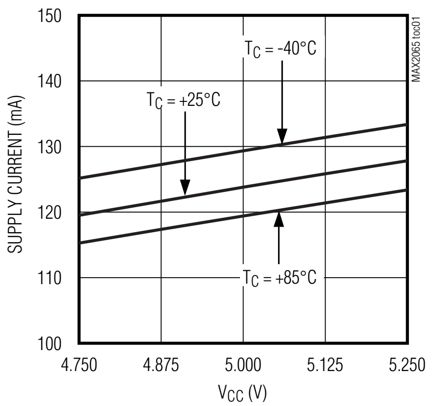
Note 5: All limits include external component losses. Output measurements are performed at RF output port of the *Typical Application Circuit*.
Note 6: Operating outside this range is possible, but with degraded performance of some parameters.
Note 7: Guaranteed by design and characterization.
Note 8: It is advisable not to operate continuously the VGA RF input above +15dBm.

50MHz to 1000MHz High-Linearity, Serial/ Parallel-Controlled Analog/Digital VGA

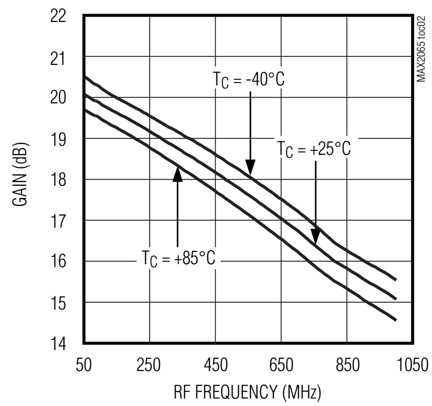
Typical Operating Characteristics

(V_{CC} = +5.0V, HC mode, both attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

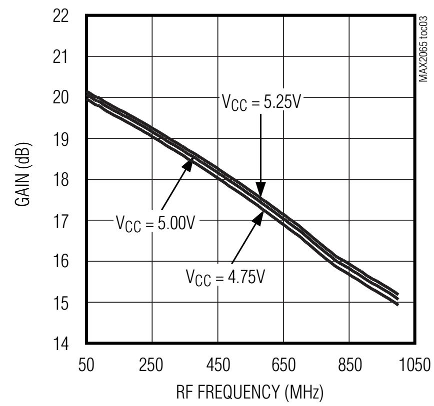
SUPPLY CURRENT vs. V_{CC}



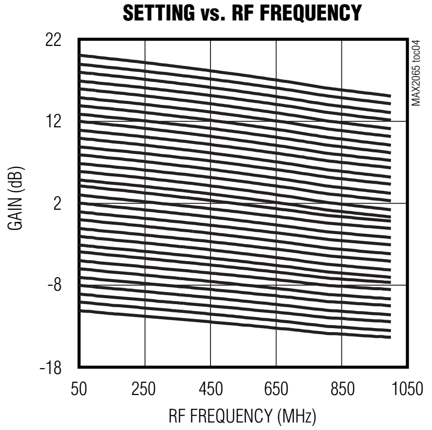
GAIN vs. RF FREQUENCY



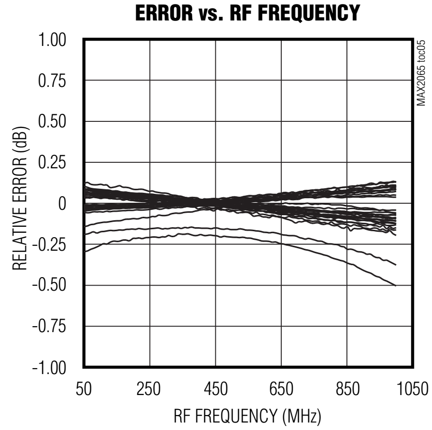
GAIN vs. RF FREQUENCY



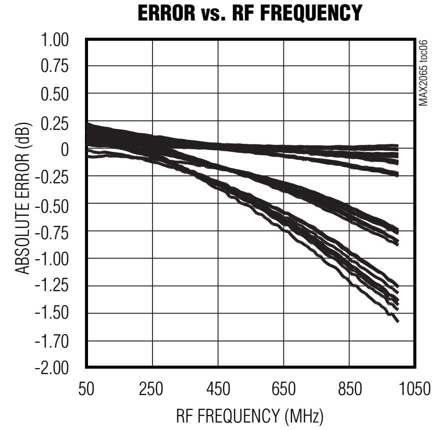
GAIN OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



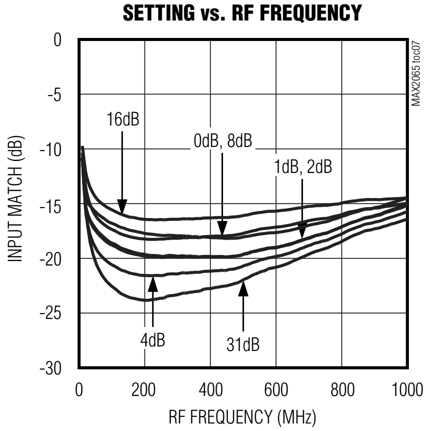
DIGITAL ATTENUATOR RELATIVE ERROR vs. RF FREQUENCY



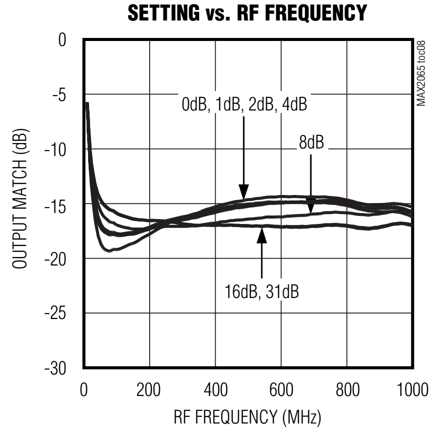
DIGITAL ATTENUATOR ABSOLUTE ERROR vs. RF FREQUENCY



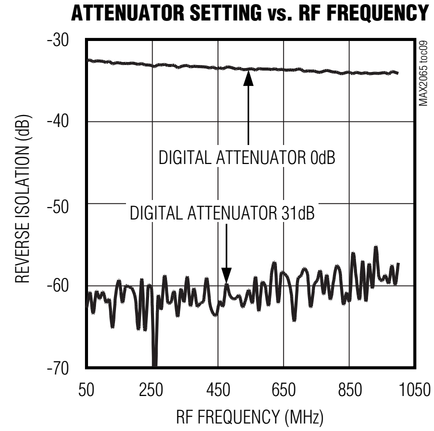
INPUT MATCH OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



OUTPUT MATCH OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



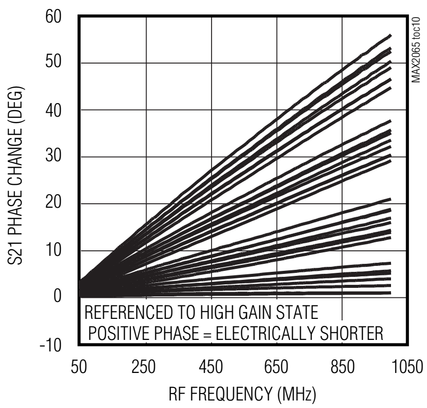
REVERSE ISOLATION OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



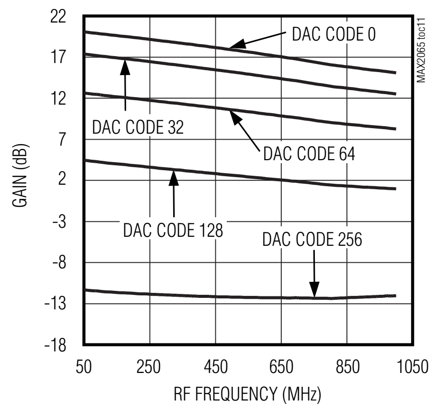
Typical Operating Characteristics (continued)

(**V_{CC} = +5.0V, HC mode**, both attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

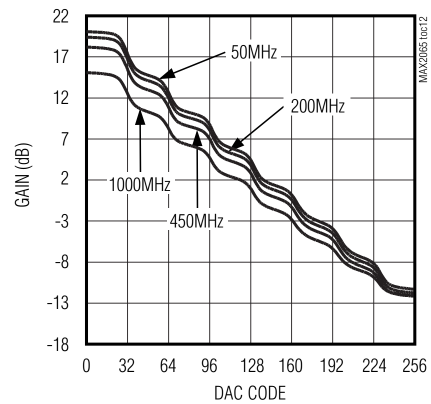
S21 PHASE CHANGE OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



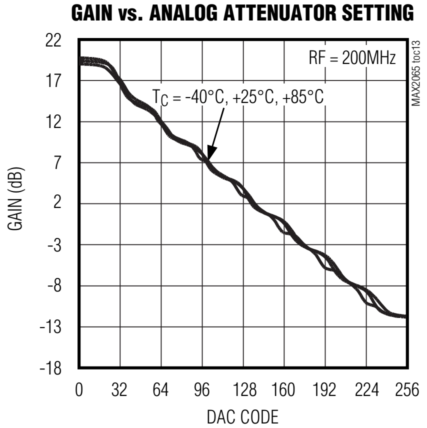
GAIN OVER ANALOG ATTENUATOR SETTING vs. RF FREQUENCY



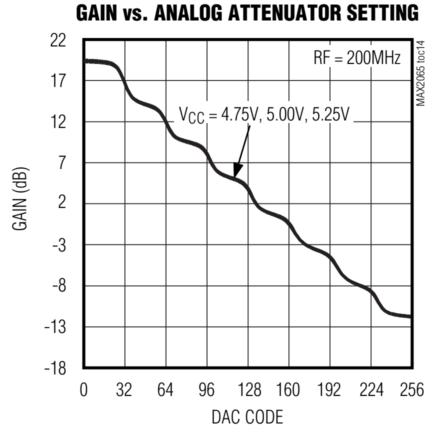
GAIN vs. ANALOG ATTENUATOR SETTING



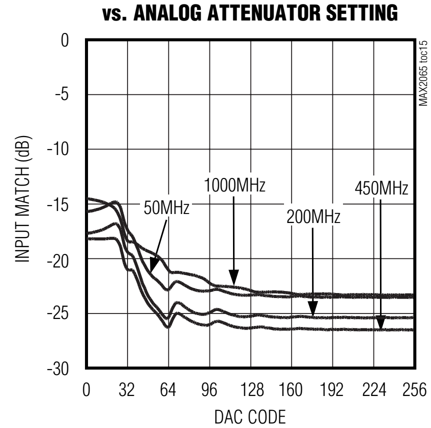
GAIN vs. ANALOG ATTENUATOR SETTING



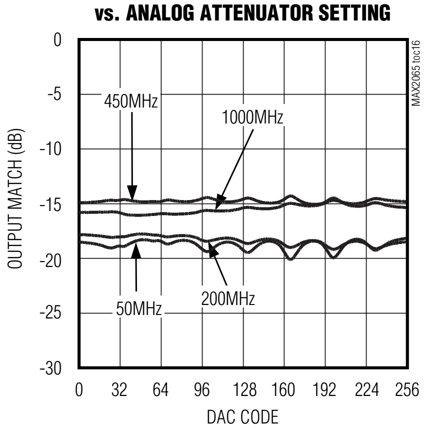
GAIN vs. ANALOG ATTENUATOR SETTING



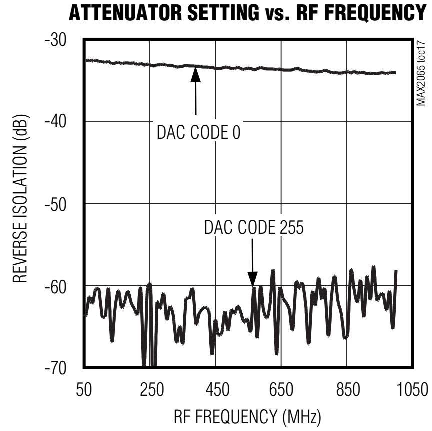
INPUT MATCH vs. ANALOG ATTENUATOR SETTING



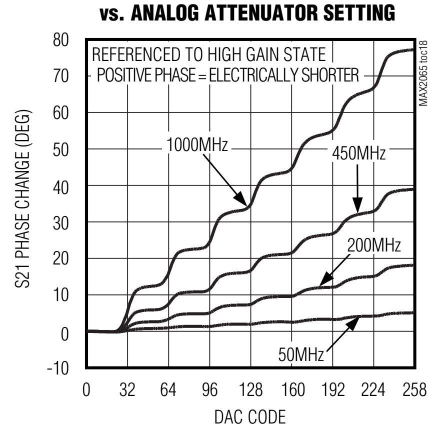
OUTPUT MATCH vs. ANALOG ATTENUATOR SETTING



REVERSE ISOLATION OVER ANALOG ATTENUATOR SETTING vs. RF FREQUENCY



S21 PHASE CHANGE vs. ANALOG ATTENUATOR SETTING

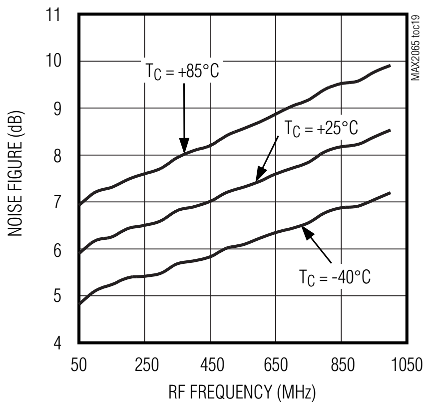


50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Analog/Digital VGA

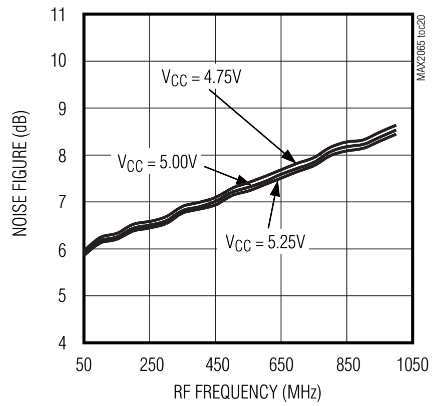
Typical Operating Characteristics (continued)

(**V_{CC} = +5.0V, HC mode**, both attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

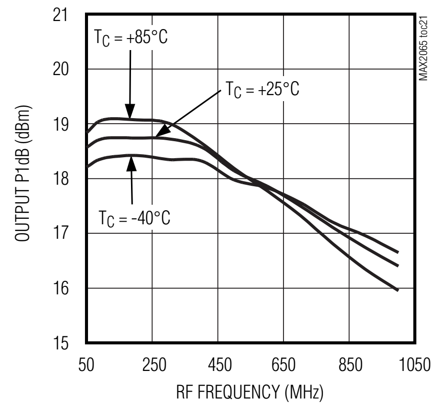
NOISE FIGURE vs. RF FREQUENCY



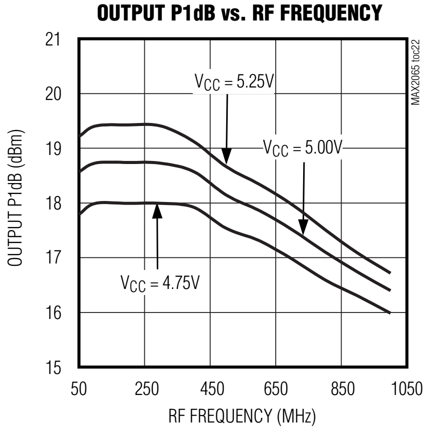
NOISE FIGURE vs. RF FREQUENCY



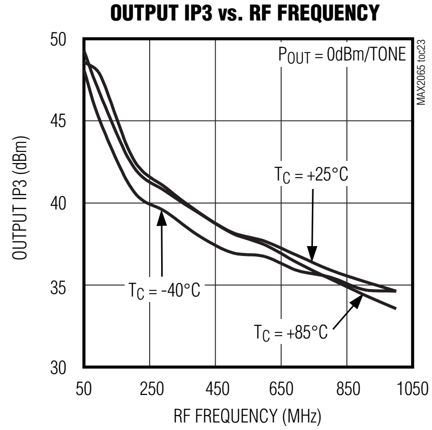
OUTPUT P1dB vs. RF FREQUENCY



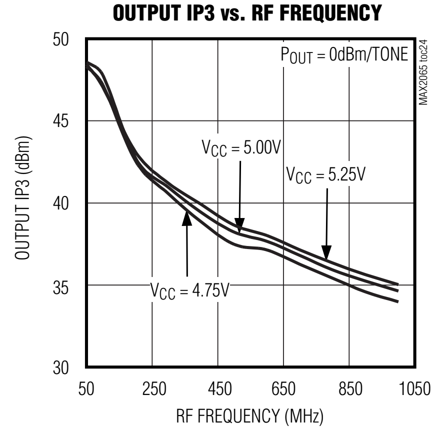
OUTPUT P1dB vs. RF FREQUENCY



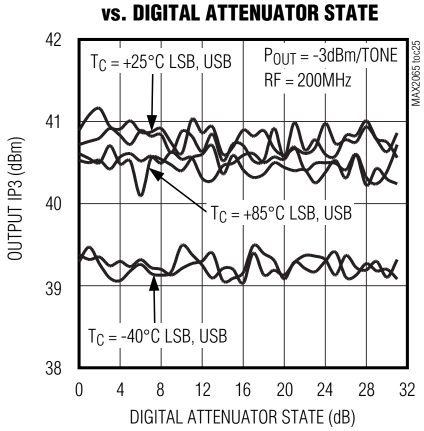
OUTPUT IP3 vs. RF FREQUENCY



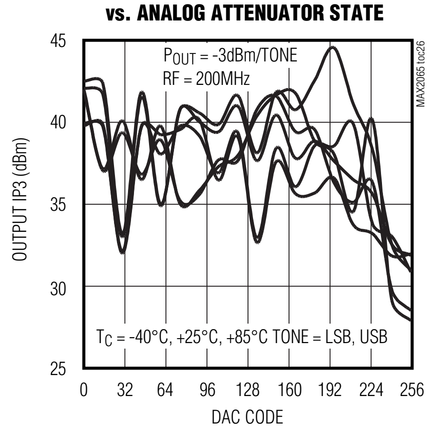
OUTPUT IP3 vs. RF FREQUENCY



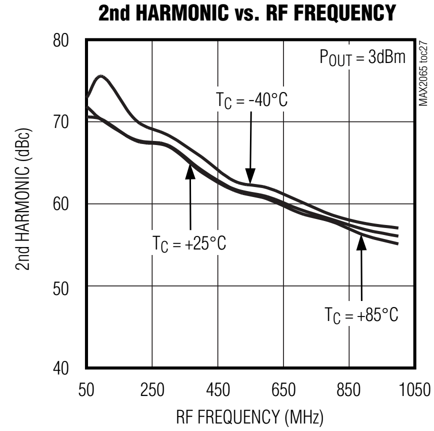
OUTPUT IP3 vs. DIGITAL ATTENUATOR STATE



OUTPUT IP3 vs. ANALOG ATTENUATOR STATE



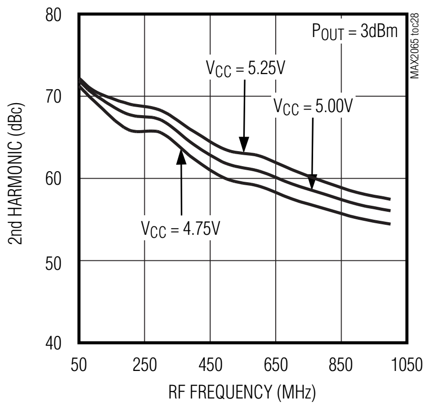
2nd HARMONIC vs. RF FREQUENCY



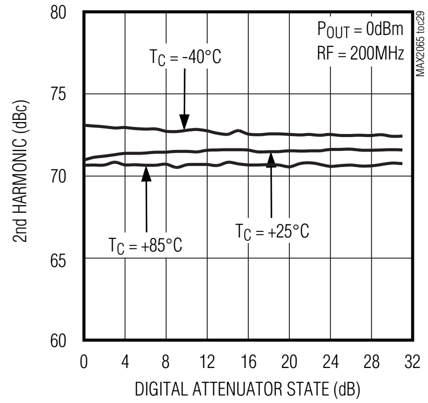
Typical Operating Characteristics (continued)

(**V_{CC} = +5.0V, HC mode**, both attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

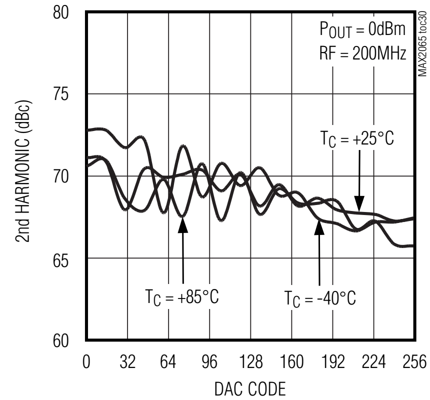
2nd HARMONIC vs. RF FREQUENCY



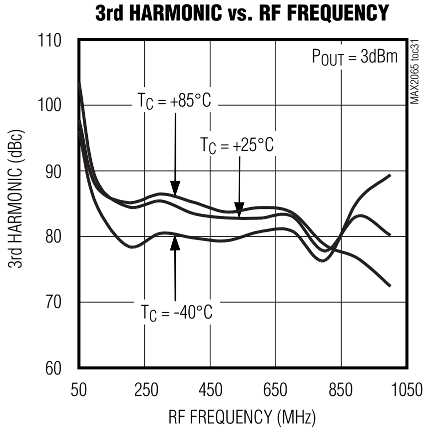
2nd HARMONIC vs. DIGITAL ATTENUATOR STATE



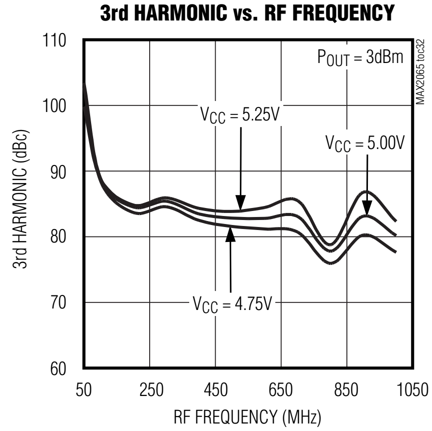
2nd HARMONIC vs. ANALOG ATTENUATOR STATE



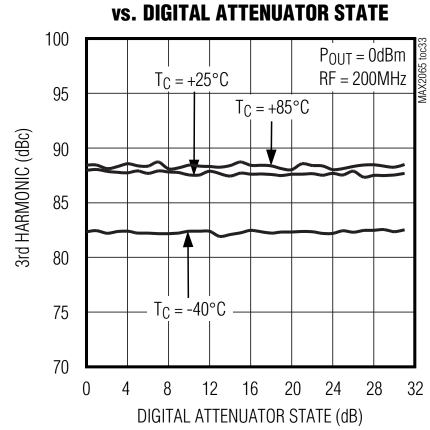
3rd HARMONIC vs. RF FREQUENCY



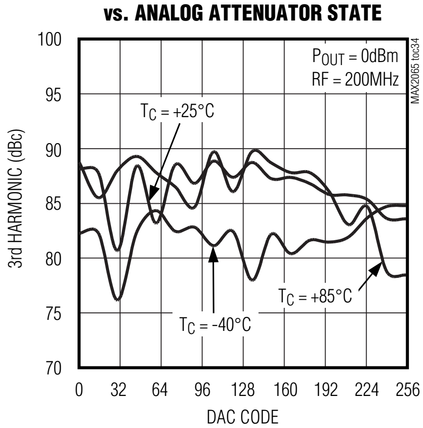
3rd HARMONIC vs. RF FREQUENCY



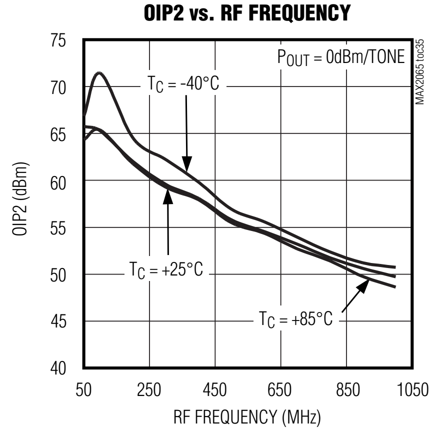
3rd HARMONIC vs. DIGITAL ATTENUATOR STATE



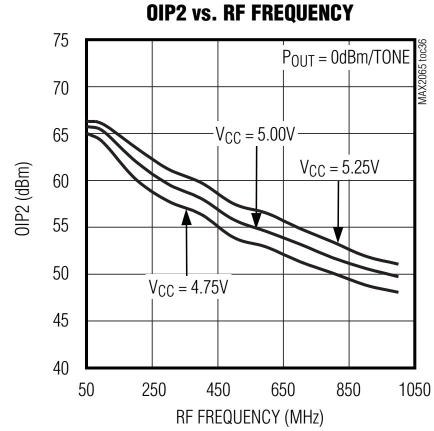
3rd HARMONIC vs. ANALOG ATTENUATOR STATE



OIP2 vs. RF FREQUENCY



OIP2 vs. RF FREQUENCY

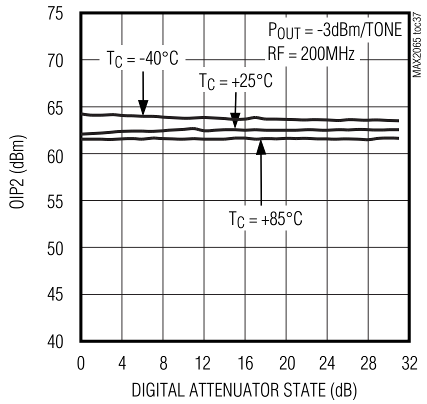


50MHz to 1000MHz High-Linearity, Serial/ Parallel-Controlled Analog/Digital VGA

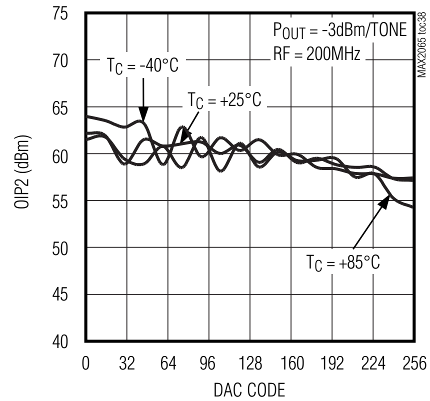
Typical Operating Characteristics (continued)

(**V_{CC} = +5.0V, HC mode**, both attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

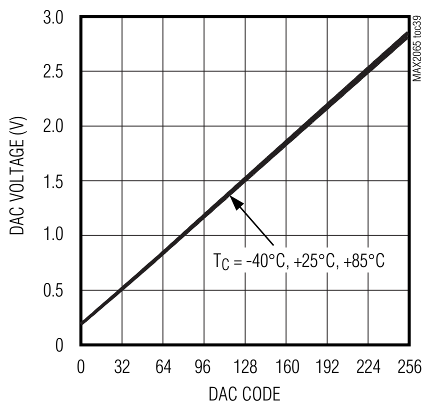
OIP2 vs. DIGITAL ATTENUATOR STATE



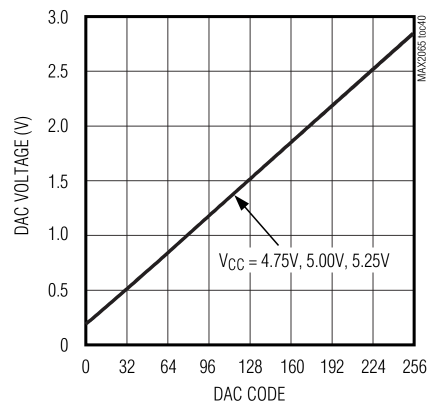
OIP2 vs. ANALOG ATTENUATOR STATE



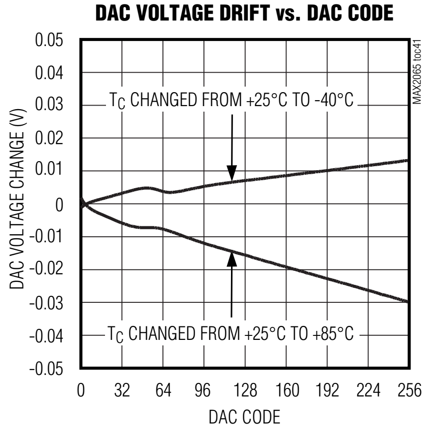
DAC VOLTAGE vs. DAC CODE



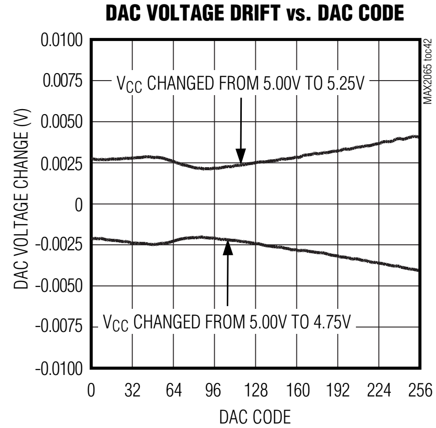
DAC VOLTAGE vs. DAC CODE



DAC VOLTAGE DRIFT vs. DAC CODE

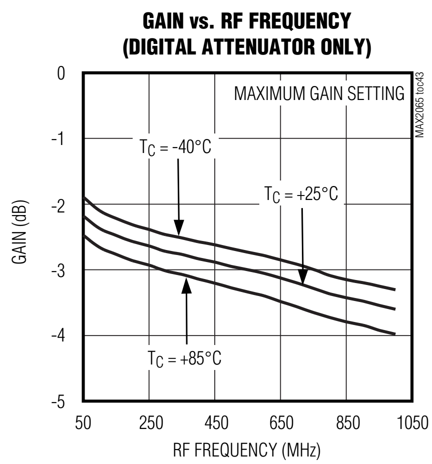


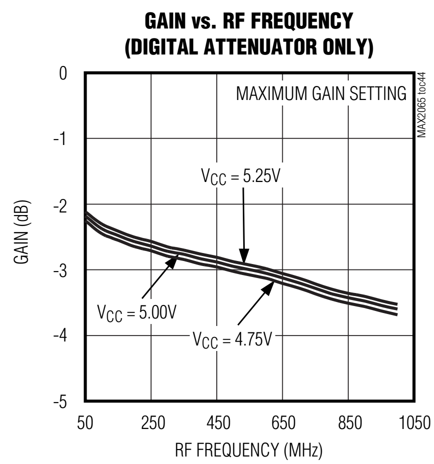
DAC VOLTAGE DRIFT vs. DAC CODE

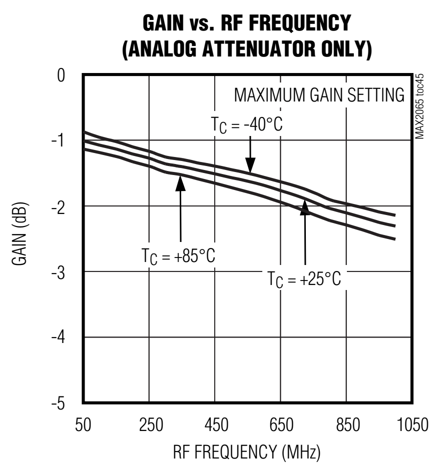


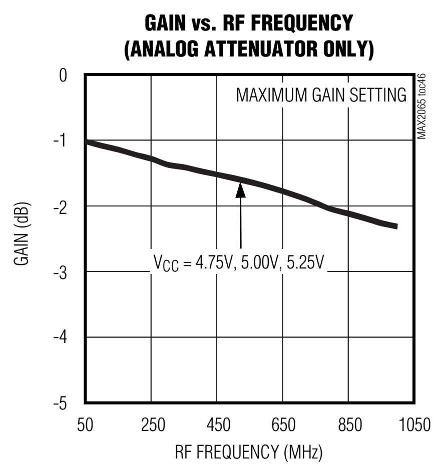
Typical Operating Characteristics (continued)

(**V_{CC} = +5.0V, attenuator only**, maximum gain, P_{IN} = -20dBm and T_C = +25°C, unless otherwise noted.)





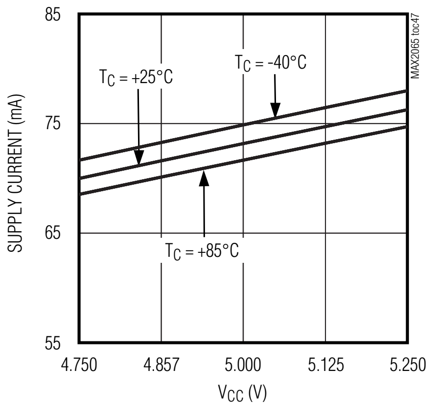




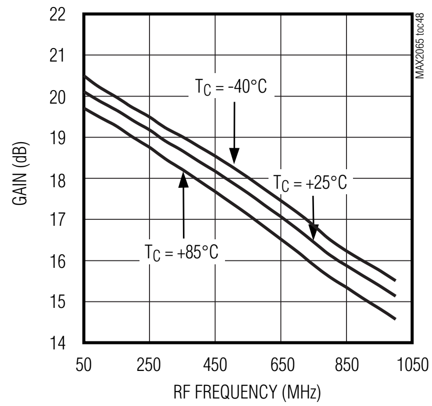
Typical Operating Characteristics (continued)

(V_{CC} = +5.0V, LC mode, both attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal reference used, unless otherwise noted.)

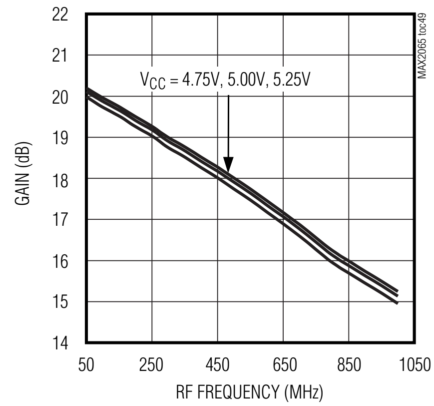
SUPPLY CURRENT vs. V_{CC} (LOW CURRENT MODE)



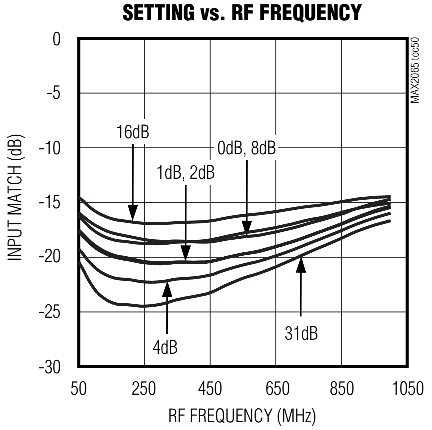
GAIN vs. RF FREQUENCY (LOW CURRENT MODE)



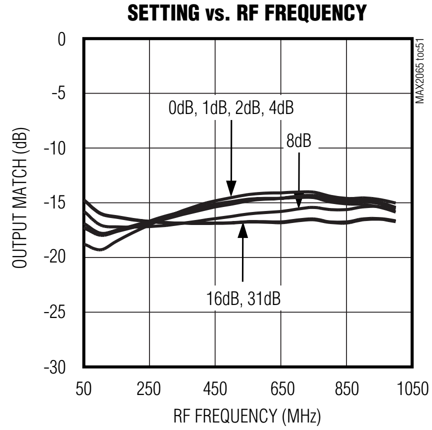
GAIN vs. RF FREQUENCY (LOW CURRENT MODE)



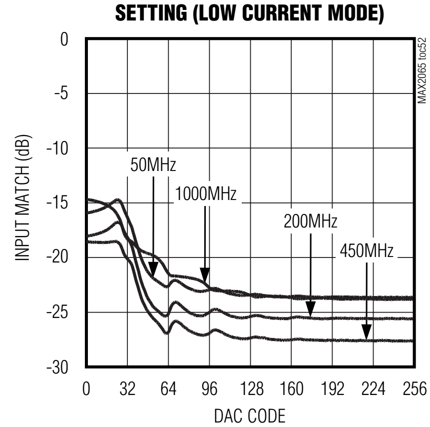
INPUT MATCH OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



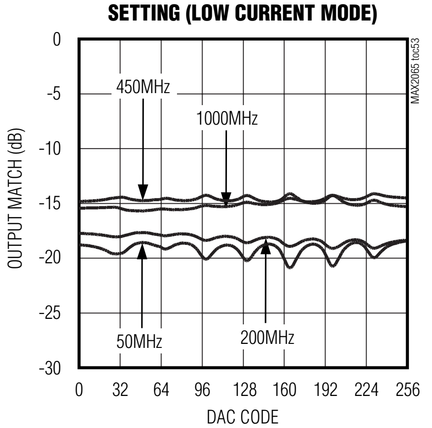
OUTPUT MATCH OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



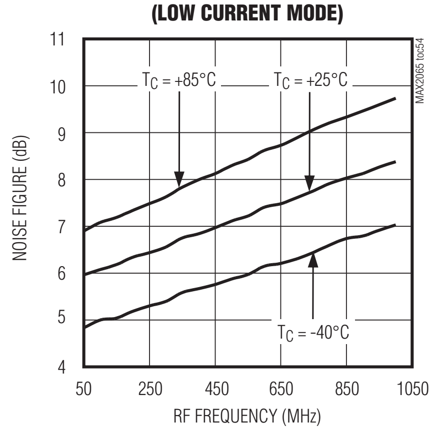
INPUT MATCH vs. ANALOG ATTENUATOR SETTING (LOW CURRENT MODE)



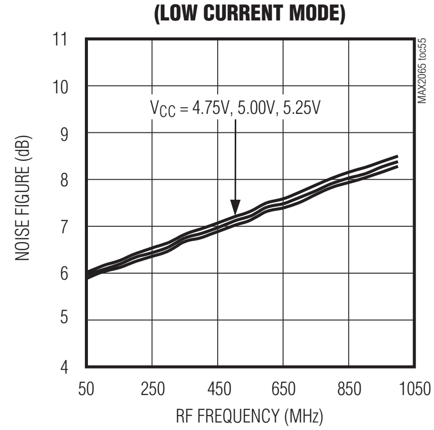
OUTPUT MATCH vs. ANALOG ATTENUATOR SETTING (LOW CURRENT MODE)



NOISE FIGURE vs. RF FREQUENCY (LOW CURRENT MODE)



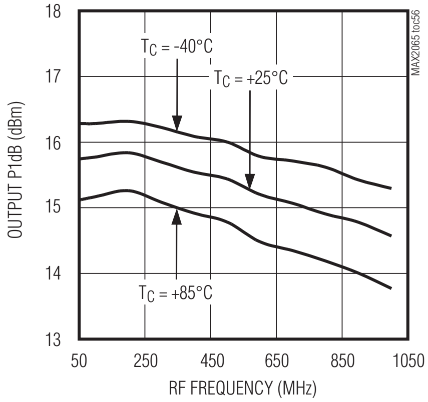
NOISE FIGURE vs. RF FREQUENCY (LOW CURRENT MODE)



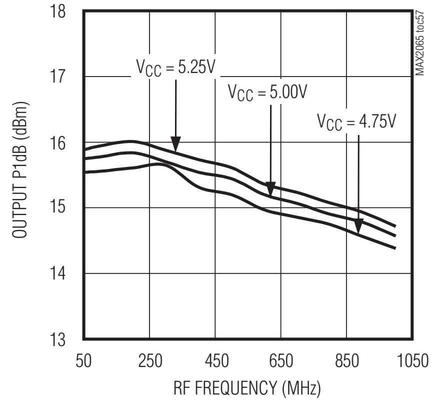
Typical Operating Characteristics (continued)

(V_{CC} **= +5.0V, LC mode**, both attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal reference used, unless otherwise noted.)

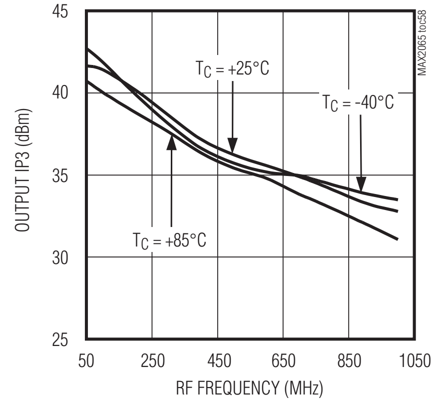
OUTPUT P1dB vs. RF FREQUENCY (LOW CURRENT MODE)



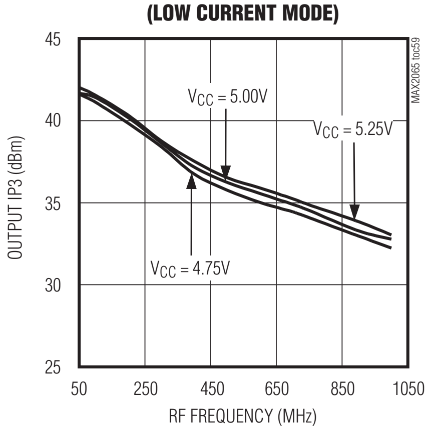
OUTPUT P1dB vs. RF FREQUENCY (LOW CURRENT MODE)



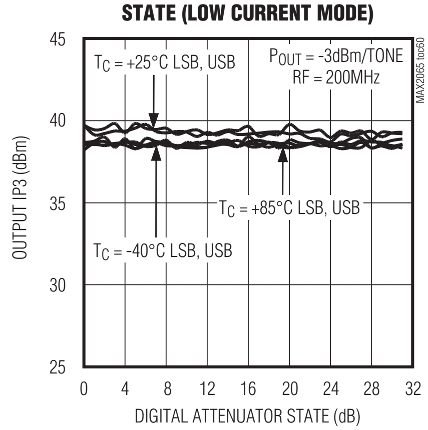
OUTPUT IP3 vs. RF FREQUENCY (LOW CURRENT MODE)



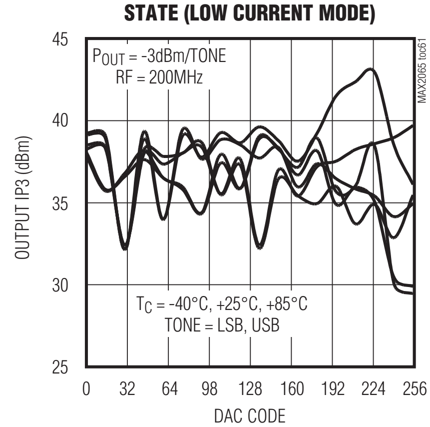
OUTPUT IP3 vs. RF FREQUENCY (LOW CURRENT MODE)



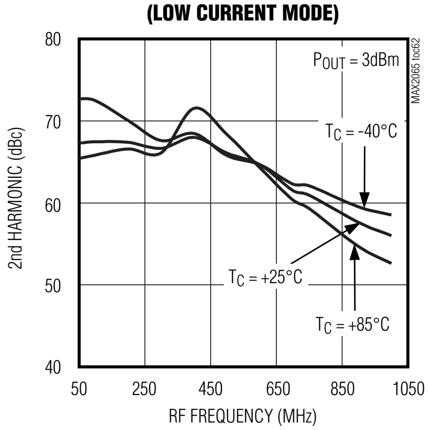
OUTPUT IP3 vs. DIGITAL ATTENUATOR STATE (LOW CURRENT MODE)



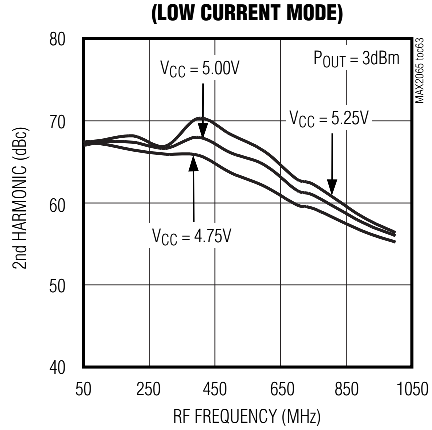
OUTPUT IP3 vs. ANALOG ATTENUATOR STATE (LOW CURRENT MODE)



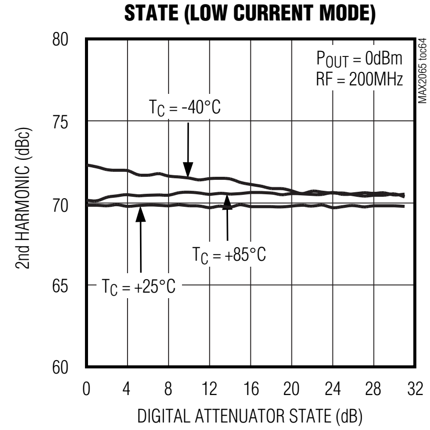
2nd HARMONIC vs. RF FREQUENCY (LOW CURRENT MODE)



2nd HARMONIC vs. RF FREQUENCY (LOW CURRENT MODE)



2nd HARMONIC vs. DIGITAL ATTENUATOR STATE (LOW CURRENT MODE)

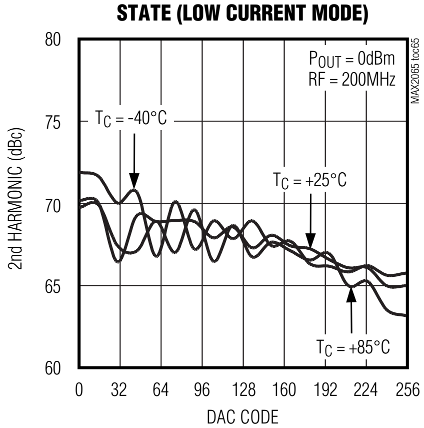


50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Analog/Digital VGA

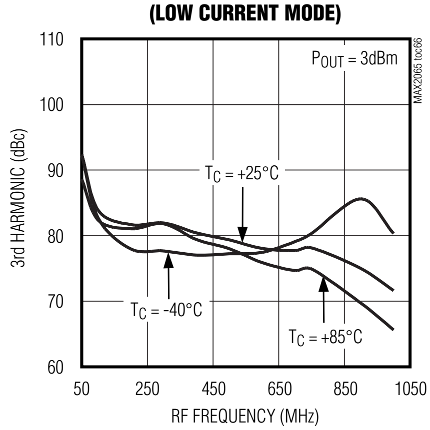
Typical Operating Characteristics (continued)

(V_{CC} **= +5.0V, LC mode**, both attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal reference used, unless otherwise noted.)

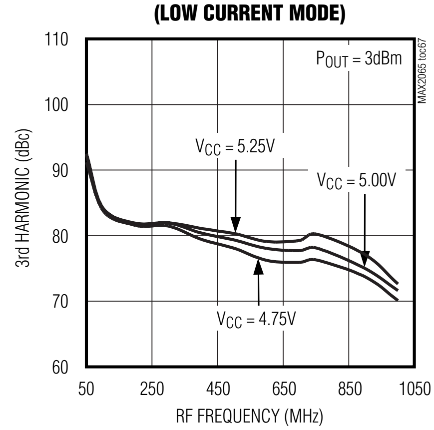
2nd HARMONIC vs. ANALOG ATTENUATOR STATE (LOW CURRENT MODE)



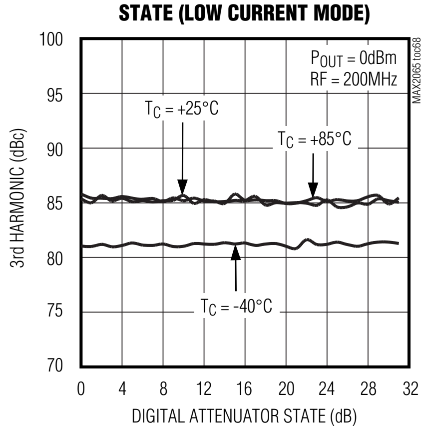
3rd HARMONIC vs. RF FREQUENCY (LOW CURRENT MODE)



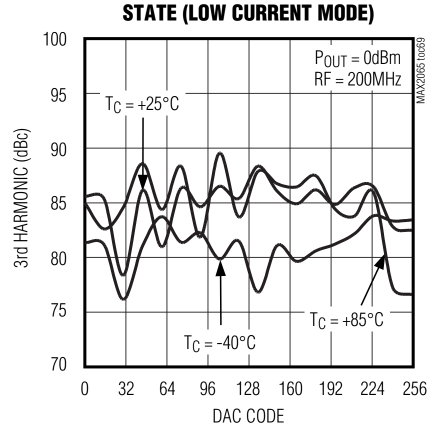
3rd HARMONIC vs. RF FREQUENCY (LOW CURRENT MODE)



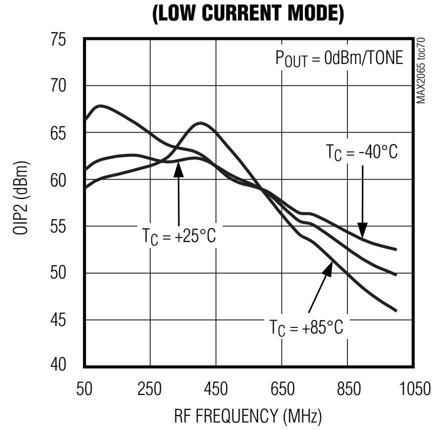
3rd HARMONIC vs. DIGITAL ATTENUATOR STATE (LOW CURRENT MODE)



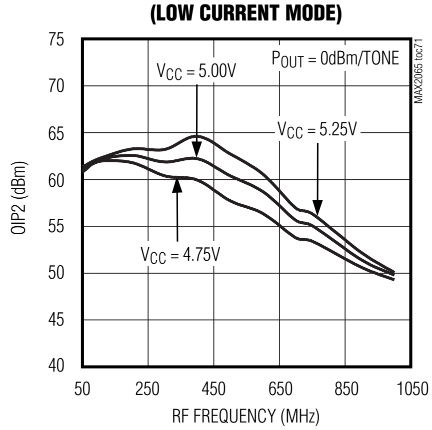
3rd HARMONIC vs. ANALOG ATTENUATOR STATE (LOW CURRENT MODE)



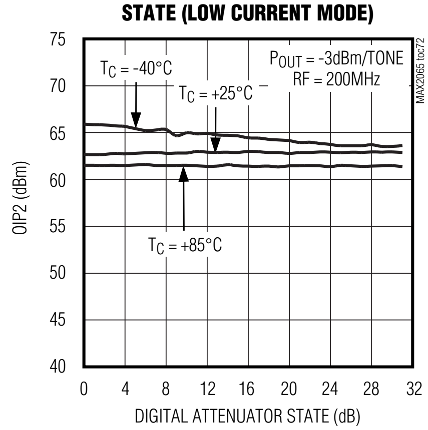
OIP2 vs. RF FREQUENCY (LOW CURRENT MODE)



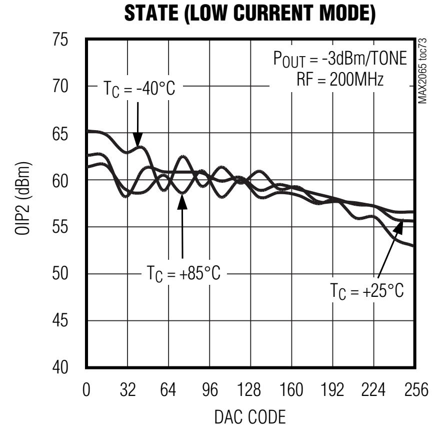
OIP2 vs. RF FREQUENCY (LOW CURRENT MODE)



OIP2 vs. DIGITAL ATTENUATOR STATE (LOW CURRENT MODE)



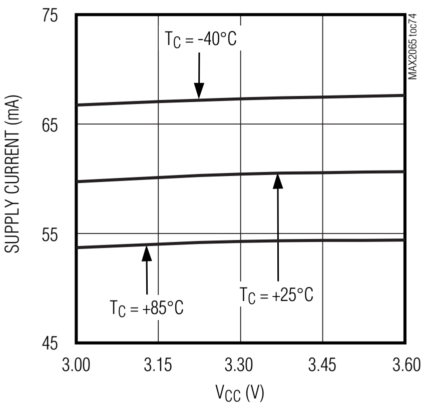
OIP2 vs. ANALOG ATTENUATOR STATE (LOW CURRENT MODE)



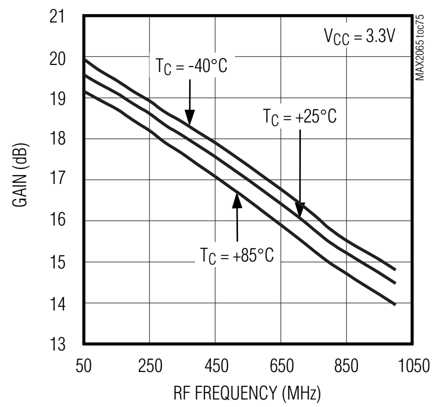
Typical Operating Characteristics (continued)

(**V_{CC} = +3.3V, HC mode**, both attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

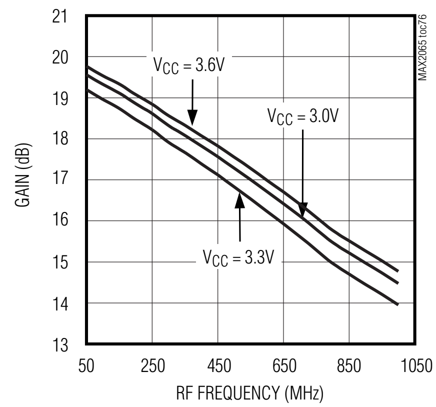
SUPPLY CURRENT vs. V_{CC}



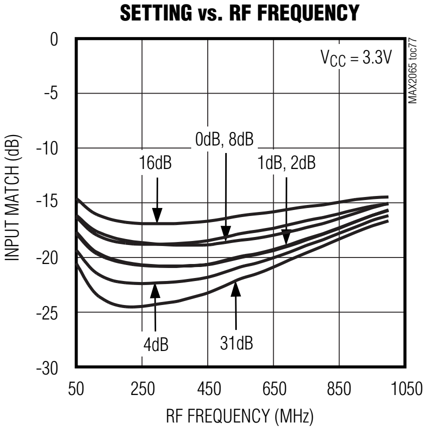
GAIN vs. RF FREQUENCY



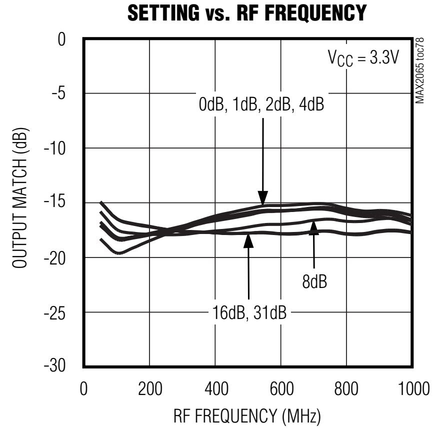
GAIN vs. RF FREQUENCY



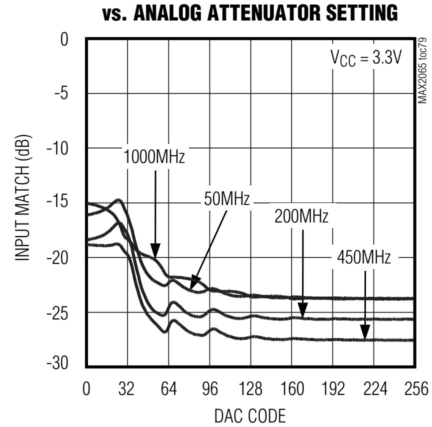
INPUT MATCH OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



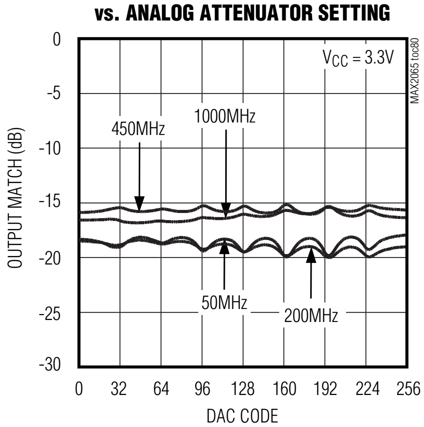
OUTPUT MATCH OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



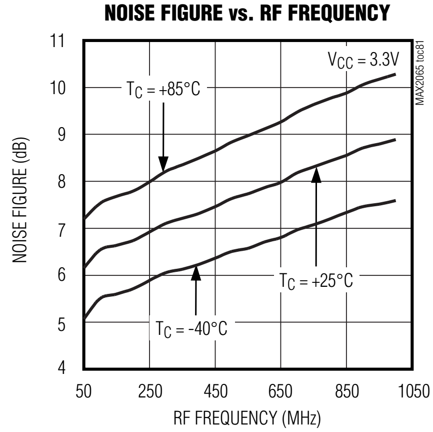
INPUT MATCH vs. ANALOG ATTENUATOR SETTING



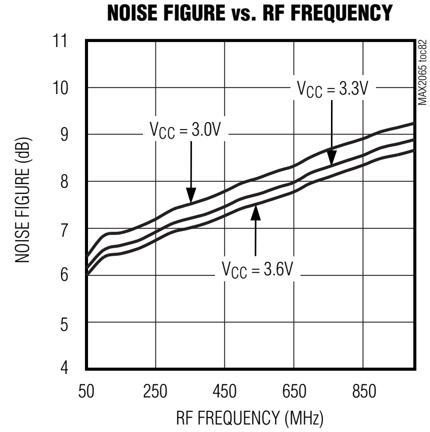
OUTPUT MATCH vs. ANALOG ATTENUATOR SETTING



NOISE FIGURE vs. RF FREQUENCY



NOISE FIGURE vs. RF FREQUENCY

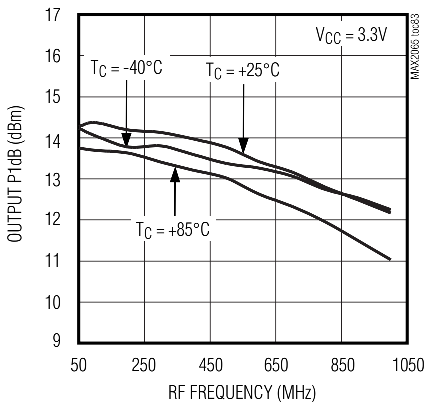


50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Analog/Digital VGA

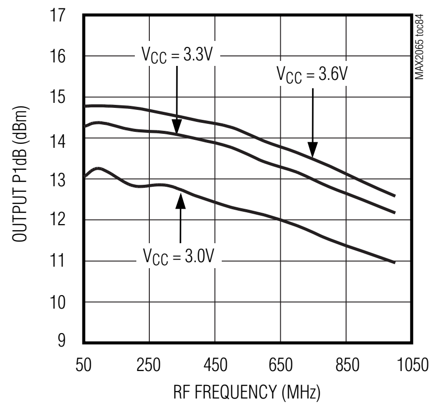
Typical Operating Characteristics (continued)

(V_{CC} **= +3.3V, HC mode**, both attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

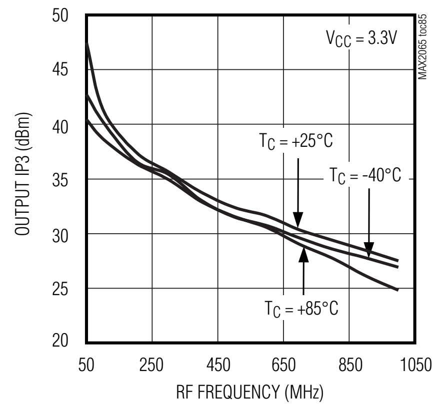
OUTPUT P1dB vs. RF FREQUENCY



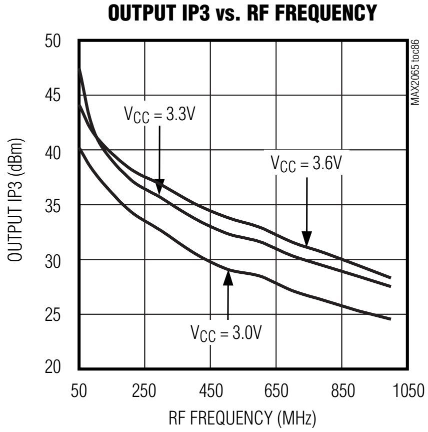
OUTPUT P1dB vs. RF FREQUENCY



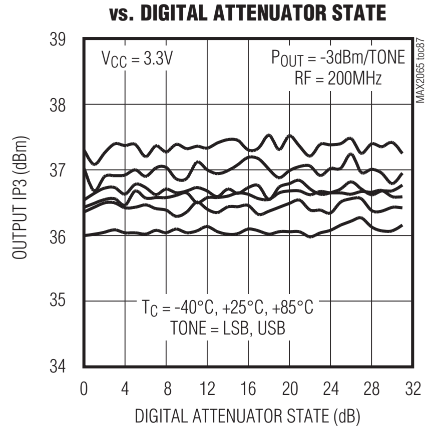
OUTPUT IP3 vs. RF FREQUENCY



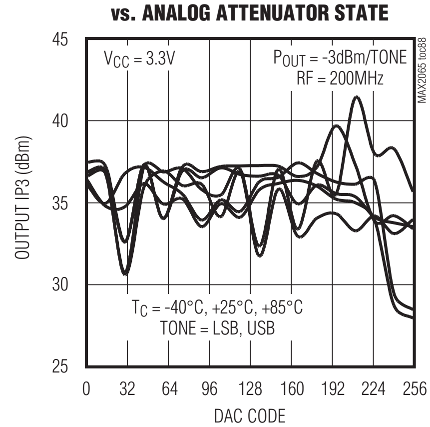
OUTPUT IP3 vs. RF FREQUENCY



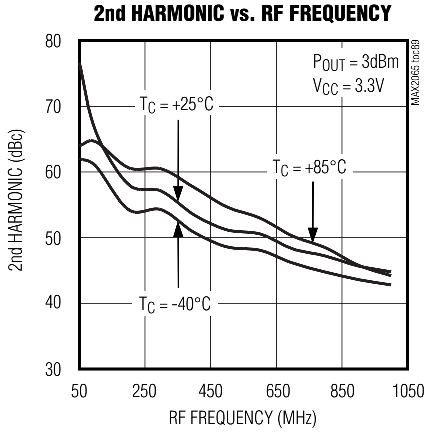
OUTPUT IP3 vs. DIGITAL ATTENUATOR STATE



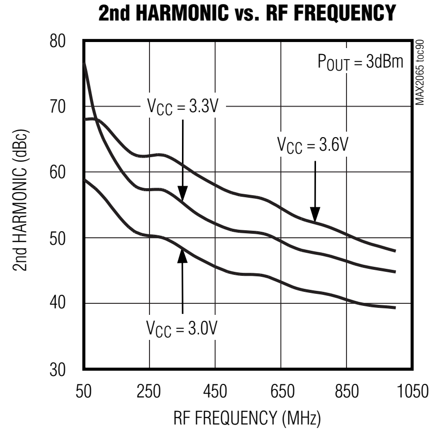
OUTPUT IP3 vs. ANALOG ATTENUATOR STATE



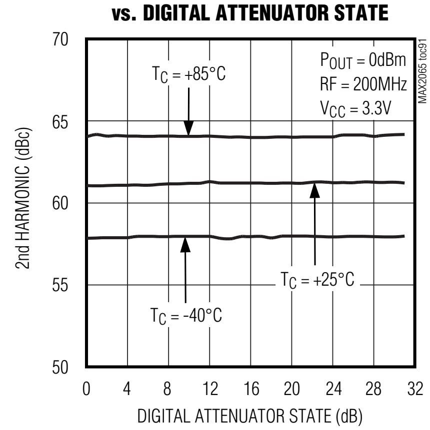
2nd HARMONIC vs. RF FREQUENCY



2nd HARMONIC vs. RF FREQUENCY



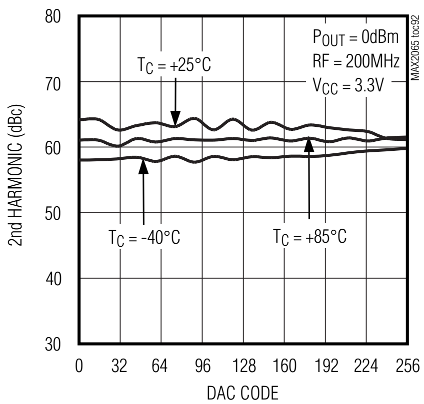
2nd HARMONIC vs. DIGITAL ATTENUATOR STATE



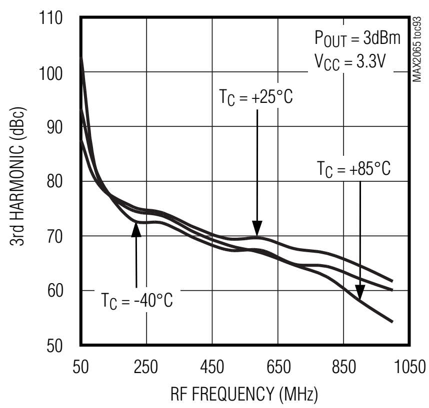
Typical Operating Characteristics (continued)

(**V_{CC} = +3.3V, HC mode**, both attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

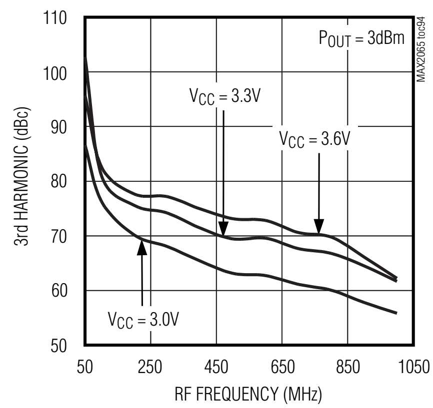
2nd HARMONIC vs. ANALOG ATTENUATOR STATE



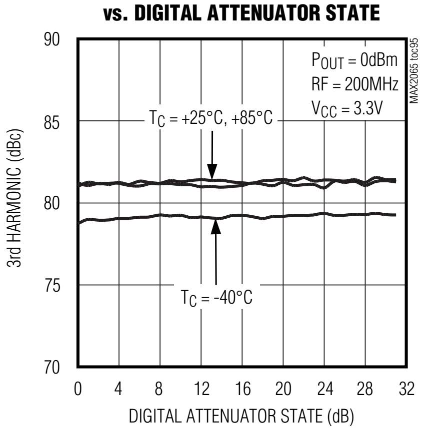
3rd HARMONIC vs. RF FREQUENCY



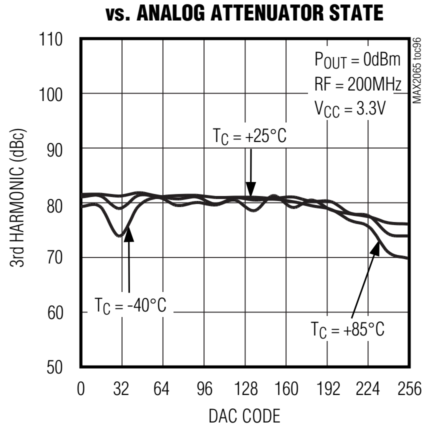
3rd HARMONIC vs. RF FREQUENCY



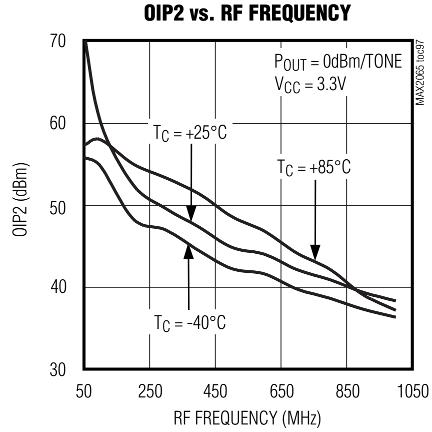
3rd HARMONIC vs. DIGITAL ATTENUATOR STATE



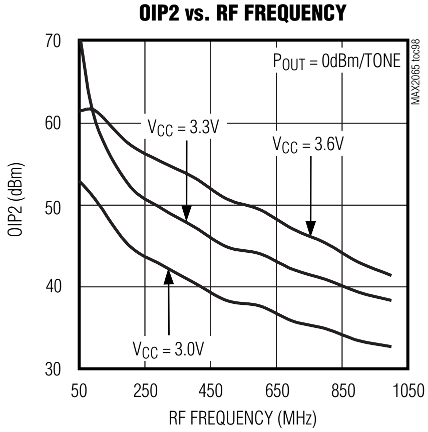
3rd HARMONIC vs. ANALOG ATTENUATOR STATE



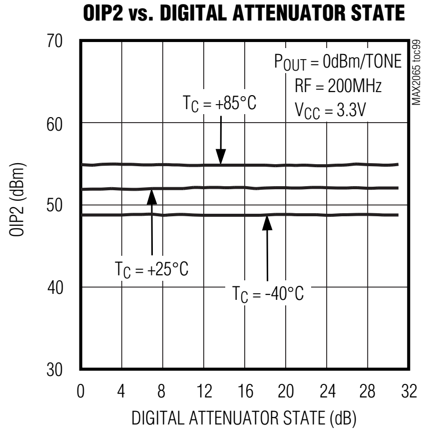
OIP2 vs. RF FREQUENCY



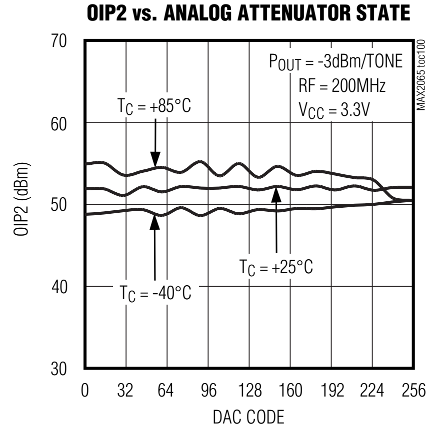
OIP2 vs. RF FREQUENCY



OIP2 vs. DIGITAL ATTENUATOR STATE



OIP2 vs. ANALOG ATTENUATOR STATE



50MHz to 1000MHz High-Linearity, Serial/ Parallel-Controlled Analog/Digital VGA

Pin Description

PIN	NAME	DESCRIPTION
1, 16, 19, 22, 24–28, 30, 31, 33–36	GND	Ground
2	VREF_SELECT	DAC Reference Voltage Selection Logic Input. Logic 1 = internal DAC reference voltage, Logic 0 = external DAC reference voltage. Logic input disabled (don't care) when VDAC_EN = Logic 0.
3	VDAC_EN	DAC Enable/Disable Logic Input. Logic 0 = disable DAC circuit, Logic 1 = enable DAC circuit.
4	DATA	SPI Data Digital Input
5	CLK	SPI Clock Digital Input
6	$\overline{CS}$	SPI Chip-Select Digital Input
7	VDD_LOGIC	Digital Logic Supply Input
8	SER/PAR	Digital Attenuator SPI or Parallel Control Selection Logic Input. Logic 0 = parallel control, Logic 1 = serial control.
9	STATE_A	Digital Attenuator Preprogrammed Attenuation State Logic Input
10	STATE_B	**State A** / **State B** / **Digital Attenuator** Logic = 0 / Logic = 0 / Preprogrammed State 1 Logic = 1 / Logic = 0 / Preprogrammed State 2 Logic = 0 / Logic = 1 / Preprogrammed State 3 Logic = 1 / Logic = 1 / Preprogrammed State 4
11	D4	16dB Attenuator Logic Input. Logic 0 = disable, Logic 1 = enable.
12	D3	8dB Attenuator Logic Input. Logic 0 = disable, Logic 1 = enable.
13	D2	4dB Attenuator Logic Input. Logic 0 = disable, Logic 1 = enable.
14	D1	2dB Attenuator Logic Input. Logic 0 = disable, Logic 1 = enable.
15	D0	1dB Attenuator Logic Input. Logic 0 = disable, Logic 1 = enable.
17	AMP_OUT	Driver Amplifier Output (50Ω)
18	RSET	Driver Amplifier Bias-Setting. See the *External Bias* section.
20	AMP_IN	Driver Amplifier Input (50Ω)
21	VCC_AMP	Driver Amplifier Supply Voltage Input
23	ATTEN2_OUT	5-Bit Digital Attenuator Output (50Ω)
29	ATTEN2_IN	5-Bit Digital Attenuator Input (50Ω)
32	ATTEN1_OUT	Analog Attenuator Output (50Ω)
37	ATTEN1_IN	Analog Attenuator Input (50Ω)
38	VCC_ANALOG	Analog Bias and Control Supply Voltage Input
39	ANALOG_VCTRL	Analog Attenuator Voltage Control Input
40	VREF_IN	External DAC Voltage Reference Input
—	EP	Exposed Pad. Internally connected to GND. Connect EP to GND for proper RF performance and enhanced thermal dissipation.

Detailed Description

The MAX2065 high-linearity analog/digital variable-gain amplifier is a general-purpose, high-performance amplifier designed to interface with 50Ω systems operating in the 50MHz to 1000MHz frequency range.

The MAX2065 integrates one digital attenuator and one analog attenuator to provide 62dB of total gain control, as well as a driver amplifier optimized to provide high gain, high IP3, low noise figure, and low power consumption. For applications that do not require high linearity, the bias current of the amplifier can be adjusted by an external resistor to further reduce power consumption.

The digital attenuator is controlled as a slave peripheral using either the SPI-compatible interface or a parallel bus with 31dB total adjustment range in 1dB steps. An added feature allows "rapid-fire" gain selection between each of the four unique steps (preprogrammed by the user through the SPI-compatible interface). The 2-pin control allows the user to quickly access any one of four customized attenuation states without reprogramming the SPI bus. The analog attenuator is controlled using an external voltage or through the SPI-compatible interface using an on-chip DAC. Because each of the three stages has its own external RF input and RF output, this component can be configured to either optimize NF (amplifier configured first), OIP3 (amplifier last), or a compromise of NF and OIP3. The device's performance features include 22dB standalone amplifier gain (amplifier only), 6.5dB NF at maximum gain (includes attenuator insertion loss for both attenuators), and a high OIP3 level of +42dBm. Each of these features makes the MAX2065 an ideal VGA for numerous receiver and transmitter applications.

In addition, the MAX2065 operates from a single +5V supply, or a single +3.3V supply with slightly reduced performance, and has adjustable bias to trade current consumption for linearity performance.

Analog and 5-Bit Digital Attenuator Control

The MAX2065 integrates one analog attenuator and one 5-bit digital attenuator to achieve a high level of dynamic range. The analog attenuator has a 31dB range and is controlled using an external voltage or through the 3-wire serial peripheral interface (SPI) using an on-chip 8-bit DAC. The digital attenuator has a 31dB control range, a 1dB step size, and is programmed through the 3-wire SPI. See the *Applications Information* section and Table 1 for attenuator programming details. The attenuators can be used for both static and dynamic power control.

Driver Amplifier

The MAX2065 includes a high-performance driver with a fixed gain of 22dB. The driver amplifier circuit is optimized for high linearity for the 50MHz to 1000MHz frequency range.

Applications Information

SPI Interface and Attenuator Settings

The digital attenuator is programmed through the 3-wire SPI/MICROWIRE™-compatible serial interface using 5-bit words. Twenty-eight bits of data are shifted in MSB first and is framed by $\overline{CS}$. When $\overline{CS}$ is low, the clock is active and data is shifted on the rising edge of the clock. When $\overline{CS}$ transitions high, the data is latched and the attenuator setting changes (Figure 1). See Table 2 for details on the SPI data format.

Table 1. Control Logic

VDAC_EN	SER/PAR	VREF_SELECT	ANALOG ATTENUATOR	DIGITAL ATTENUATOR	D/A CONVERTER
0	0	X	Controlled by external control voltage	Parallel controlled	Disabled
1	0	1	Controlled by on-chip DAC	Parallel controlled	Enabled (DAC uses on-chip voltage reference)
0	1	X	Controlled by external control voltage	SPI controlled	Disabled
1	1	0	Controlled by on-chip DAC	SPI controlled	Enabled (DAC uses external voltage reference)

X = Don't care.

MICROWIRE is a trademark of National Semiconductor Corp.

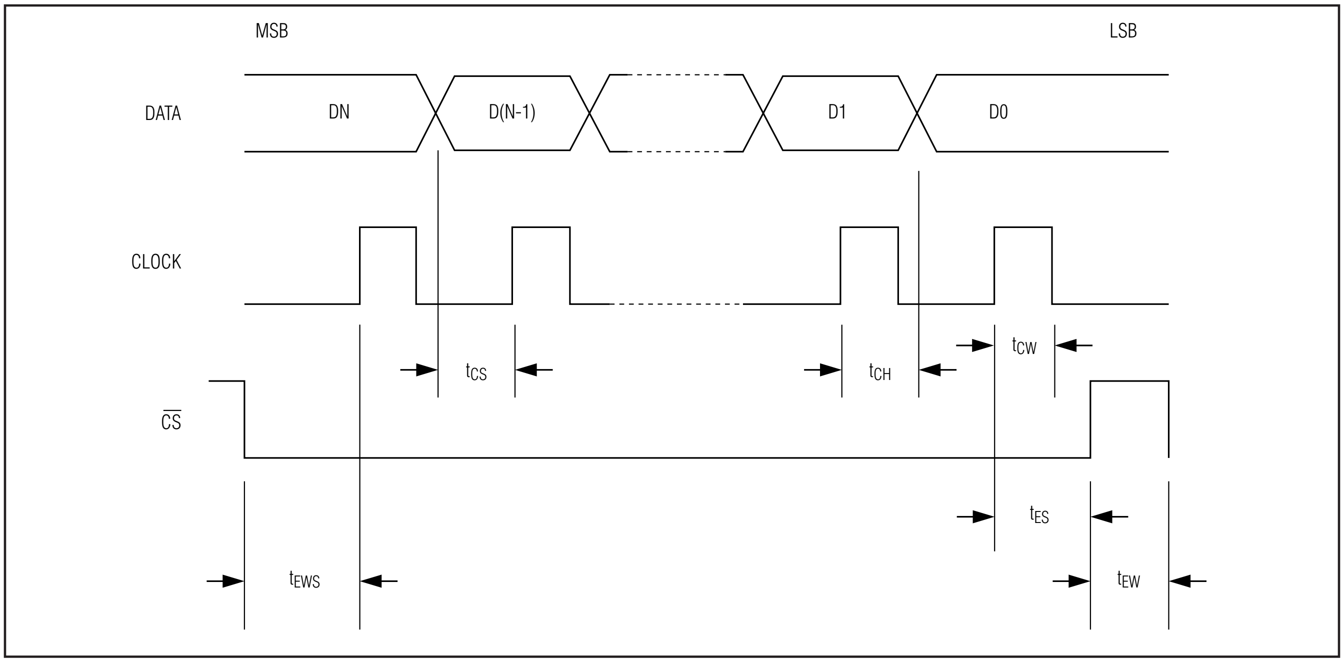


Figure 1. MAX2065 SPI Timing Diagram

Table 2. SPI Data Format

FUNCTION	BIT	DESCRIPTION
Digital Attenuator State 4	D27 (MSB)	16dB step (MSB of the 5-bit word used to program the digital attenuator state 4)
	D26	8dB step
	D25	4dB step
	D24	2dB step
	D23	1dB step (LSB)
Digital Attenuator State 3	D22	5-bit word used to program the digital attenuator state 3 (see the description for digital attenuator state 4)
	D21	
	D20	
	D19	
	D18	
Digital Attenuator State 2	D17	5-bit word used to program the digital attenuator state 2 (see the description for digital attenuator state 4)
	D16	
	D15	
	D14	
	D13	
Digital Attenuator State 1	D12	5-bit word used to program the digital attenuator state 1 (see the description for digital attenuator state 4)
	D11	
	D10	
	D9	
	D8	

Table 2. SPI Data Format (continued)

FUNCTION	BIT	DESCRIPTION
On-Chip DAC	D7	Bit 7 (MSB) of on-chip DAC used to program the analog attenuator
	D6	Bit 6 of DAC
	D5	Bit 5 of DAC
	D4	Bit 4 of DAC
	D3	Bit 3 of DAC
	D2	Bit 2 of DAC
	D1	Bit 1 of DAC
	D0 (LSB)	Bit 0 (LSB) of the on-chip DAC

Attenuator and DAC Operation

The analog attenuator is controlled by an external control voltage applied at ANALOG_VCTRL (pin 39) or by the on-chip 8-bit DAC, while the digital attenuator is controlled through the SPI-compatible interface or parallel bus. The DAC enable/disable logic-input pin (VDAC_EN), digital attenuator SPI or parallel control selection logic-input pin (SER/PAR), and the DAC reference voltage selection logic-input pin (VREF_SELECT) determine how the attenuators are controlled. The on-chip DAC can also be enabled or disabled. When the DAC is enabled, either the on-chip voltage reference or the external voltage reference can be selected. See Table 1 for the attenuator and DAC operation truth table.

Digital Attenuator Settings Using the Parallel Control Bus

To capitalize on its fast 25ns switching capability, the MAX2065 offers a supplemental 5-bit parallel control interface. The digital logic attenuator-control pins (D0–D4) enable the attenuator stages (Table 3).

Direct access to this 5-bit bus enables the user to avoid any programming delays associated with the SPI interface. One of the limitations of any SPI bus is the speed at which commands can be clocked into each peripheral device. By offering direct access to the 5-bit parallel interface, the user can quickly shift between digital attenuator states needed for critical “fast-attack” automatic gain control (AGC) applications.

“Rapid-Fire” Preprogrammed Attenuation States

The MAX2065 has an added feature that provides “rapid fire” gain selection between four preprogrammed attenuation steps. As with the supplemental 5-bit bus mentioned above, this “rapid fire” gain selection allows the user to quickly access any one of four customized digital attenuation states without incurring the delays associated with reprogramming the device through the SPI bus.

The switching speed is comparable to that achieved using the supplemental 5-bit parallel bus. However, by employing this specific feature, the digital attenuator I/O is further reduced by a factor of either 5 or 2.5 (5 control bits vs. 1 or 2, respectively) depending on the number of states desired.

Table 3. Digital Attenuator Settings (Parallel Control)

INPUT	LOGIC = 0 (OR GROUND)	LOGIC = 1
D0	Disable 1dB attenuator, or when SPI is default programmer	Enable 1dB attenuator
D1	Disable 2dB attenuator, or when SPI is default programmer	Enable 2dB attenuator
D2	Disable 4dB attenuator, or when SPI is default programmer	Enable 4dB attenuator
D3	Disable 8dB attenuator, or when SPI is default programmer	Enable 8dB attenuator
D4	Disable 16dB attenuator, or when SPI is default programmer	Enable 16dB attenuator

50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Analog/Digital VGA

The user can employ the STATE_A and STATE_B logic-input pins to apply each step as required (Table 4). Toggling just the STATE_A pin (one control bit) yields two preprogrammed attenuation states; toggling both the STATE_A and STATE_B pins together (two control bits) yield four preprogrammed attenuation states.

As an example, assume that the AGC application requires a static attenuation adjustment to trim out gain inconsistencies within a receiver lineup. The same AGC circuit can also be called upon to dynamically attenuate an unwanted blocker signal that could de-sense the receiver and lead to an ADC overdrive condition. In this example, the MAX2065 would be preprogrammed (through the SPI bus) with two customized attenuation states—one to address the static gain trim adjustment, the second to counter the unwanted blocker condition.

Table 4. Preprogrammed Attenuation State Settings

STATE_A	STATE_B	DIGITAL ATTENUATOR
0	0	Preprogrammed attenuation state 1
1	0	Preprogrammed attenuation state 2
0	1	Preprogrammed attenuation state 3
1	1	Preprogrammed attenuation state 4

Toggling just the STATE_A control bit enables the user to switch quickly between the static and dynamic attenuation settings with only one I/O pin.

If desired, the user can also program two additional attenuation states by using the STATE_B control bit as a second I/O pin. These two additional attenuation settings are useful for software-defined radio applications where multiple static gain settings may be needed to account for different frequencies of operation, or where multiple dynamic attenuation settings are needed to account for different blocker levels (as defined by multiple wireless standards).

Cascaded OIP3 Considerations

Due to both attenuator's finite IP3 performance, the cascaded OIP3 degrades when both attenuators are set at higher attenuation states.

External Bias

Bias currents for the driver amplifier are set and optimized through external resistors. Resistors R1 and R1A connected to RSET (pin 18) set the bias current for the amplifier. The external biasing resistor values can be increased for reduced current operation at the expense of performance.

Table 5. Typical Application Circuit Component Values (HC Mode)

DESIGNATION	VALUE	SIZE	VENDOR	DESCRIPTION
C1, C2, C7, C11	10nF	0402	Murata Mfg. Co., Ltd.	X7R
C3, C4, C6, C8, C9, C10	1000pF	0402	Murata Mfg. Co., Ltd.	C0G ceramic capacitor
C12, C13	150pF	0402	Murata Mfg. Co., Ltd.	C0G ceramic capacitor
L1	470nH	1008	Coilcraft, Inc.	1008CS-471XJLC
R1, R1A	10Ω	0402	Panasonic Corp.	1%
R2 (+3.3V applications only)	1kΩ	0402	Panasonic Corp.	1%
R3 (+3.3V applications only)	2kΩ	0402	Panasonic Corp.	1%
R4 (+5V applications and using internal DAC only)	47kΩ	0402	Panasonic Corp.	1%
U1	—	40-pin thin QFN-EP (6mm x 6mm)	Maxim Integrated Products, Inc.	MAX2065ETL+

Table 6. Typical Application Circuit Component Values (LC Mode)

DESIGNATION	VALUE	SIZE	VENDOR	DESCRIPTION
C1, C2, C7, C11	10nF	0402	Murata Mfg. Co., Ltd.	X7R
C3, C4, C6, C8, C9, C10	1000pF	0402	Murata Mfg. Co., Ltd.	C0G ceramic capacitor
C12, C13	150pF	0402	Murata Mfg. Co., Ltd.	C0G ceramic capacitor
L1	470nH	1008	Coilcraft, Inc.	1008CS-471XJLC
R1	24Ω	0402	Vishay	1%
R1A	0.01µF	0402	Murata Mfg. Co., Ltd.	X7R
R2 (+3.3V applications only)	1kΩ	0402	Panasonic Corp.	1%
R3 (+3.3V applications only)	2kΩ	0402	Panasonic Corp.	1%
R4 (+5V applications and using internal DAC only)	47kΩ	0402	Panasonic Corp.	1%
U1	—	40-pin thin QFN-EP (6mm x 6mm)	Maxim Integrated Products, Inc.	MAX2065ETL+

+5V and +3.3V Supply Voltage

The MAX2065 features an optional +3.3V supply voltage operation with slightly reduced linearity performance.

Layout Considerations

The pin configuration of the MAX2065 has been optimized to facilitate a very compact physical layout of the device and its associated discrete components.

The exposed paddle (EP) of the MAX2065's 40-pin thin QFN-EP package provides a low thermal-resistance path to the die. It is important that the PCB on which the MAX2065 is mounted be designed to conduct heat from the EP. In addition, provide the EP with a low-inductance path to electrical ground. The EP **must** be soldered to a ground plane on the PCB, either directly or through an array of plated via holes.

Amplitude Overshoot Reduction

To reduce amplitude overshoot during digital attenuator state change, connect a bandpass filter (parallel LC type) from ATTEN2_OUT (pin 23) to ground. L = 18nH and C = 47pF are recommended for 169MHz operation (Figure 2). Contact the factory for recommended components for other operating frequencies.

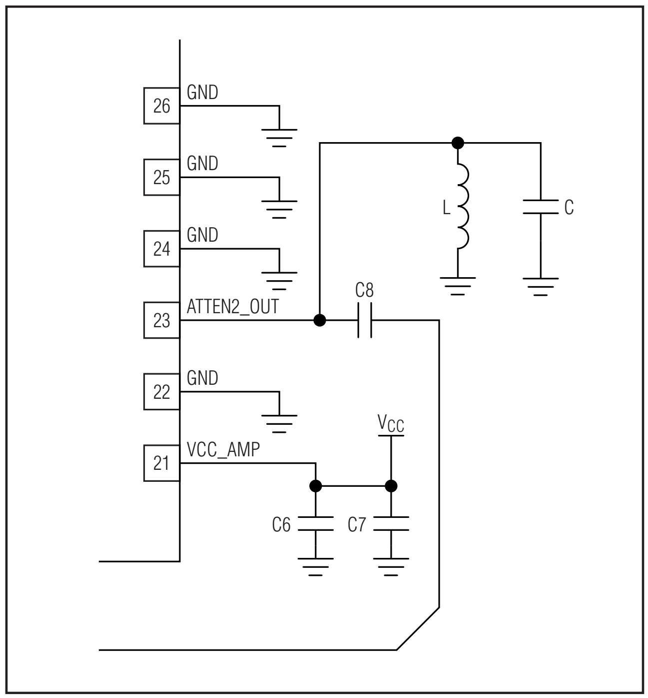
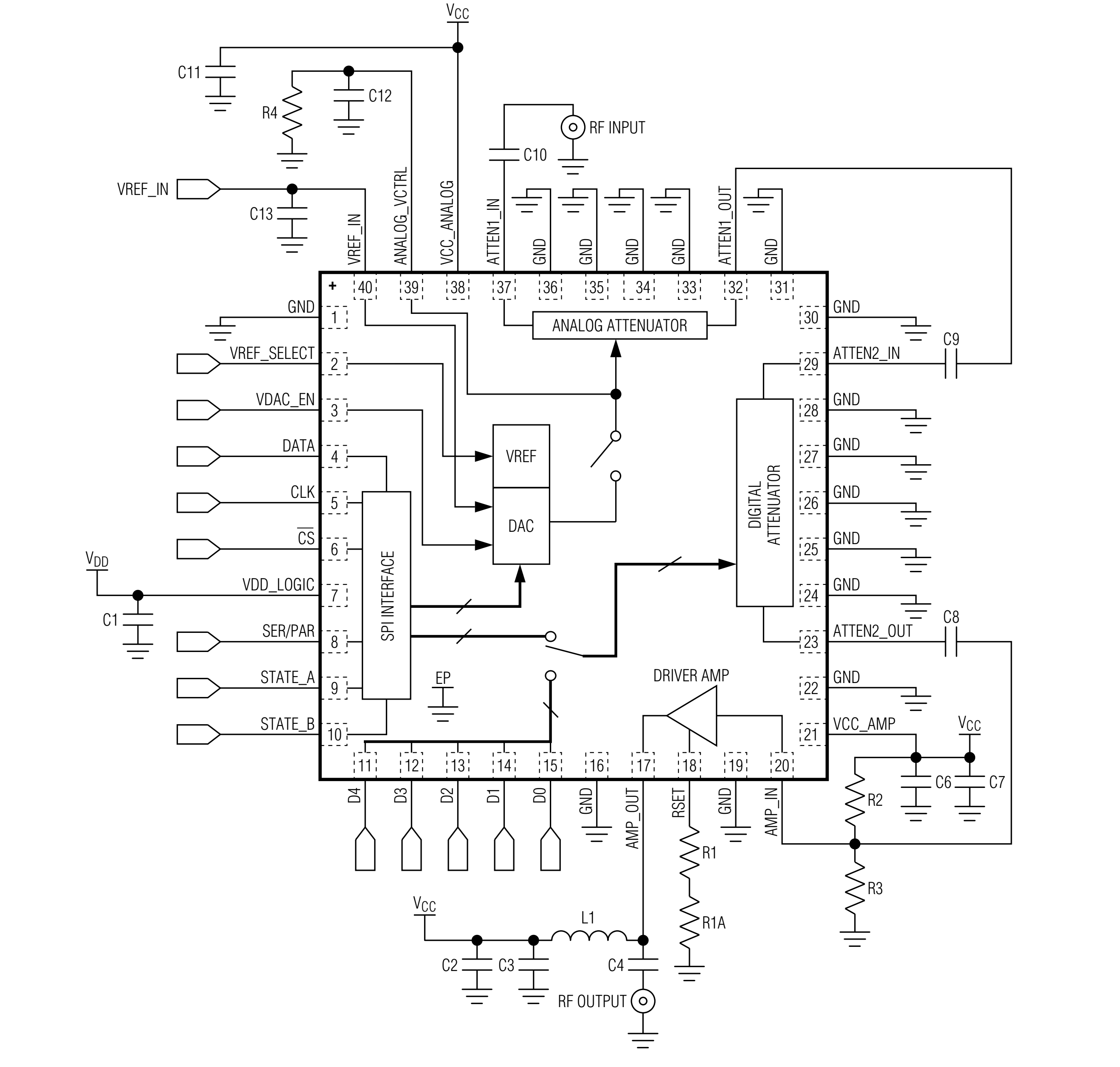


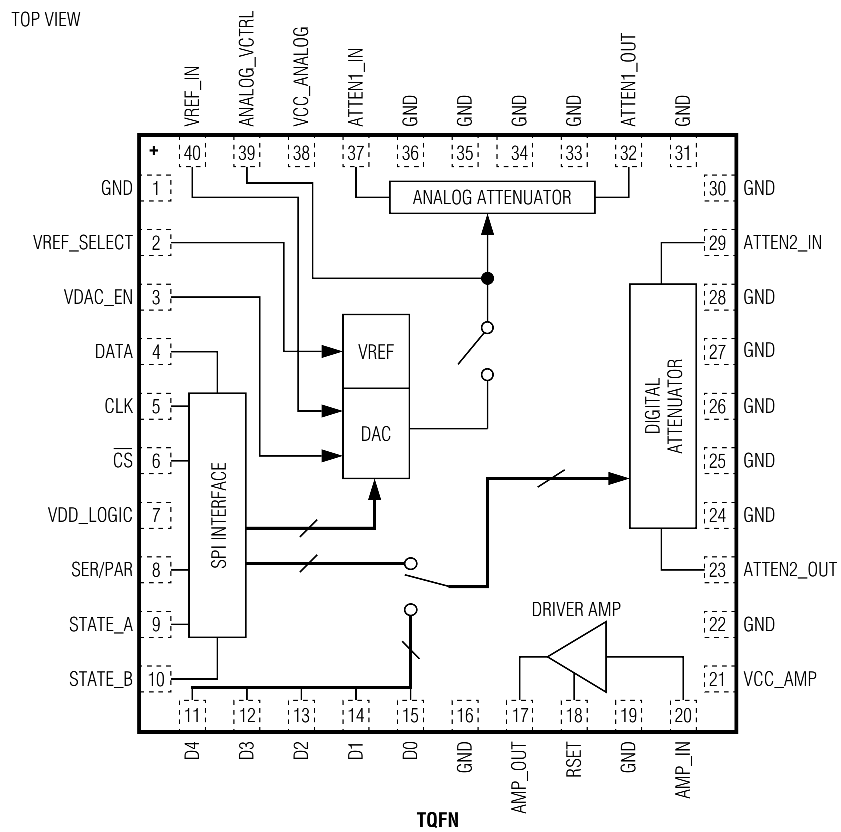
Figure 2. Bandpass Filter to Reduce Amplitude Overshoot

50MHz to 1000MHz High-Linearity, Serial/ Parallel-Controlled Analog/Digital VGA

Typical Application Circuit



Pin Configuration/Functional Block Diagram



TQFN
EXPOSED PADDLE ON BOTTOM.
CONNECT EP TO GND.

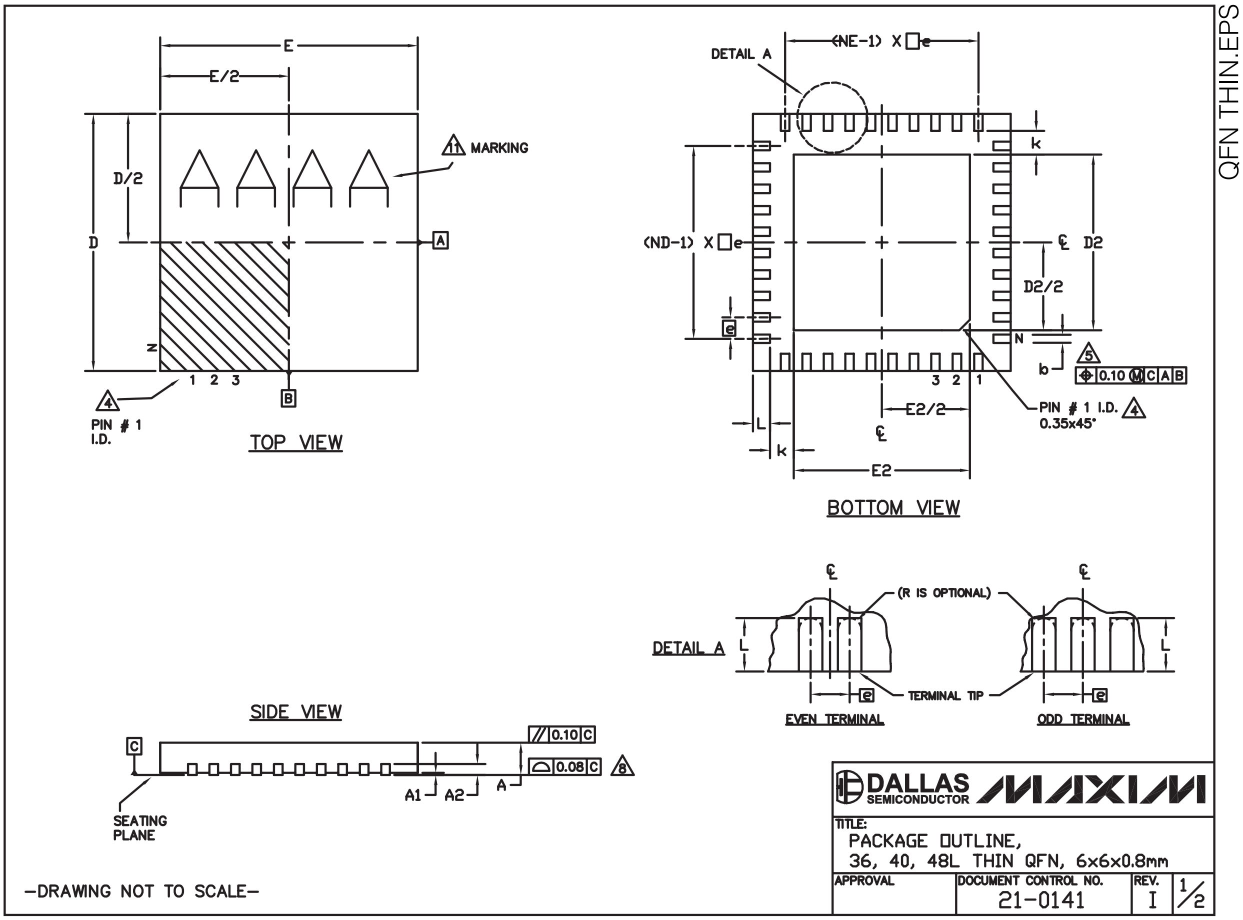
Chip Information

PROCESS: SiGe BiCMOS

50MHz to 1000MHz High-Linearity, Serial/ Parallel-Controlled Analog/Digital VGA

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Analog/Digital VGA

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–
L	0.35	0.50	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80
T3666N-1	3.60	3.70	3.80	3.60	3.70	3.80
T3666MN-1	3.60	3.70	3.80	3.60	3.70	3.80
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20
T4866-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866N-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866-2	4.40	4.50	4.60	4.40	4.50	4.60

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN FOR REFERENCE ONLY.
13. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 36, 40, 48L THIN QFN, 6x6x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0141	I	2/2